

PG600-B02 NI GHTHAWK

GB3B-384, 6GB GDDR5 128Mx32

DP + HDMI /DP + DP + DP + DVI -I

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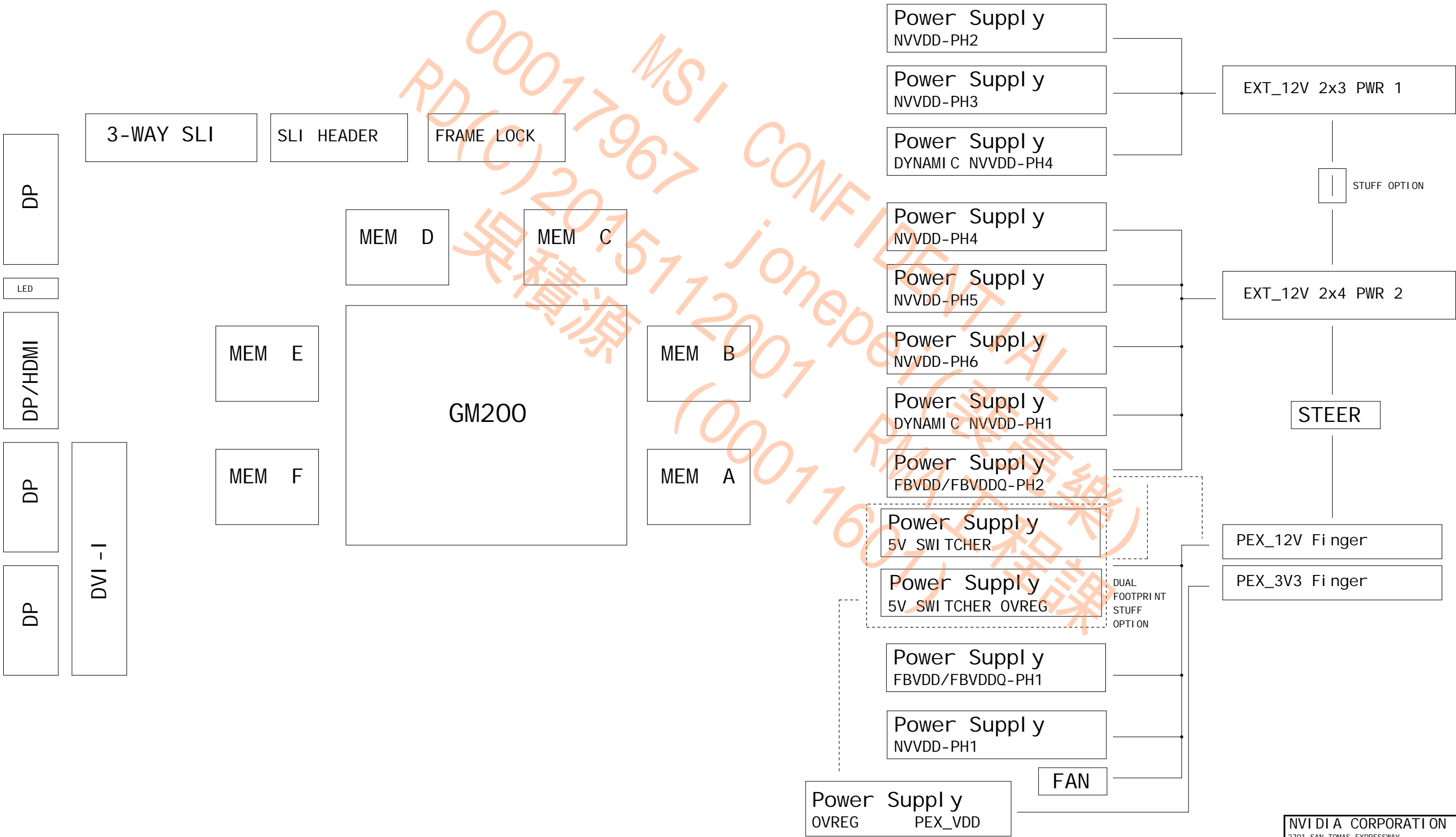
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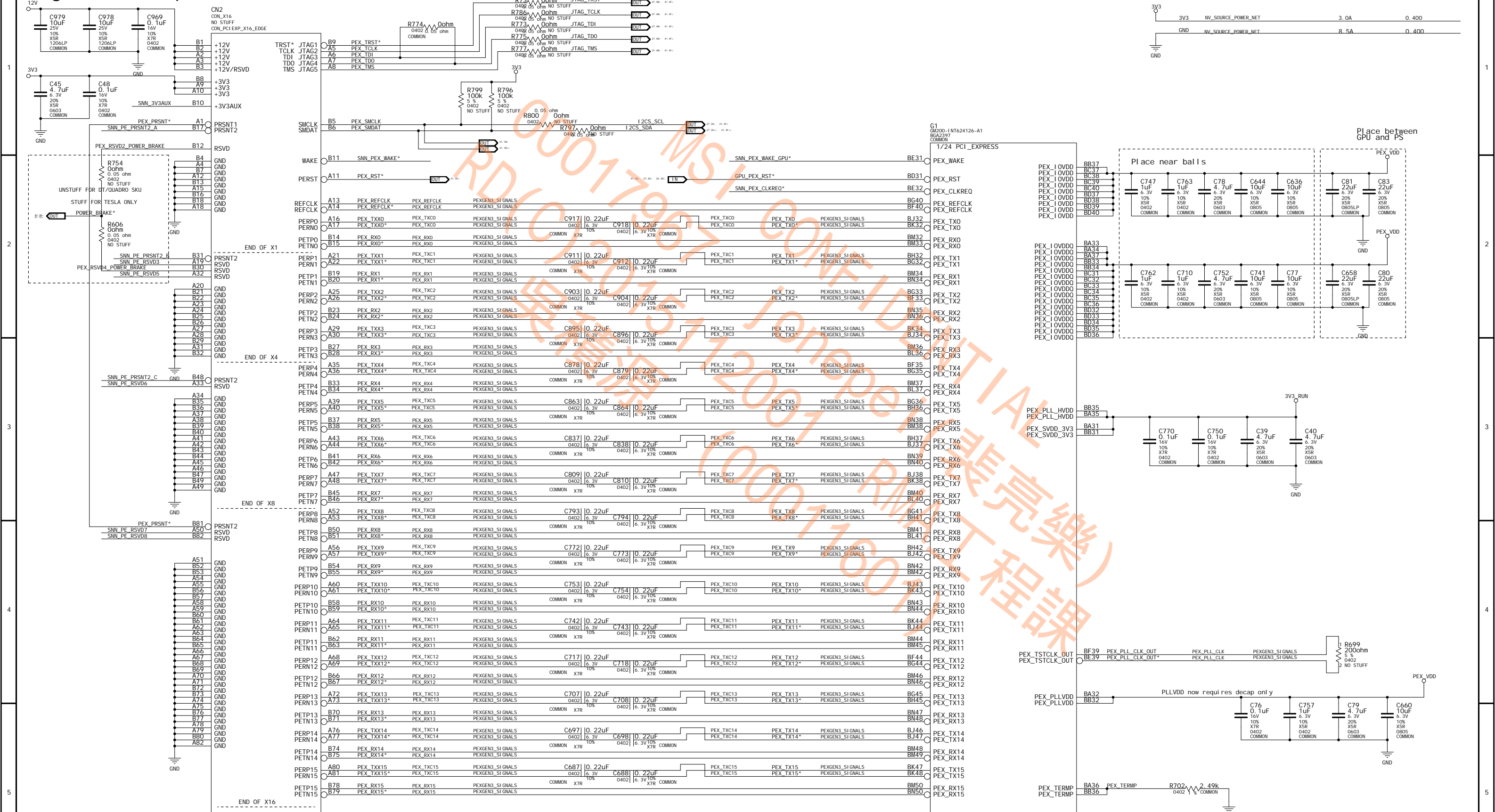


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PAGE DETAIL	PCI Express

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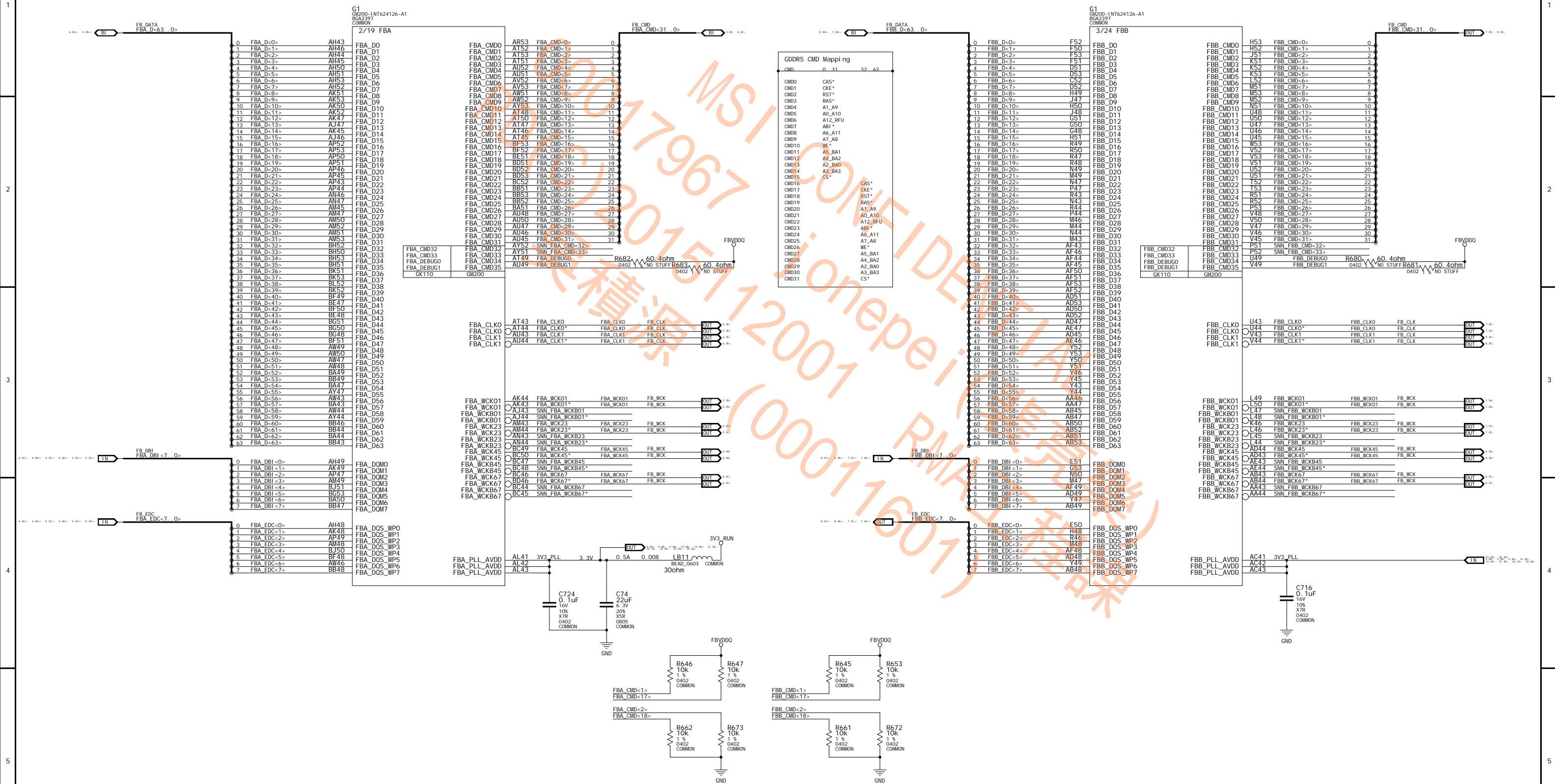


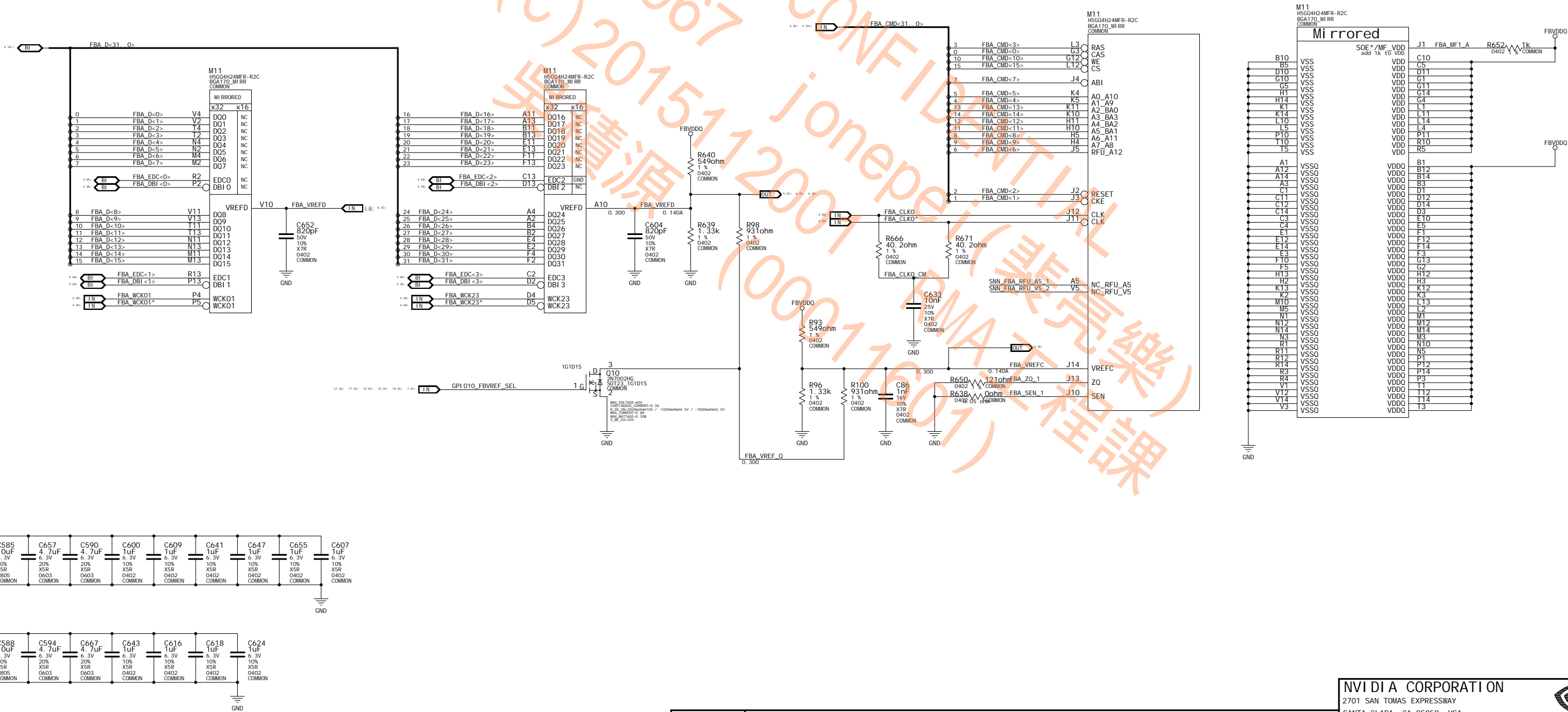
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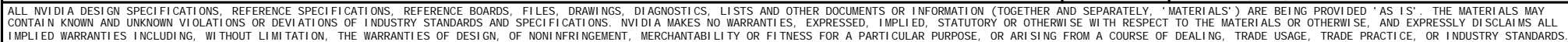
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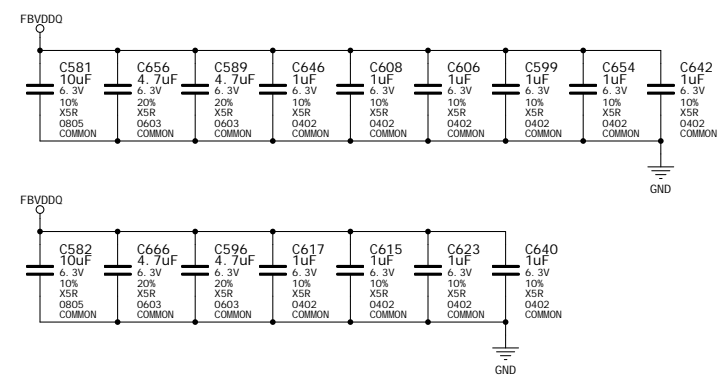
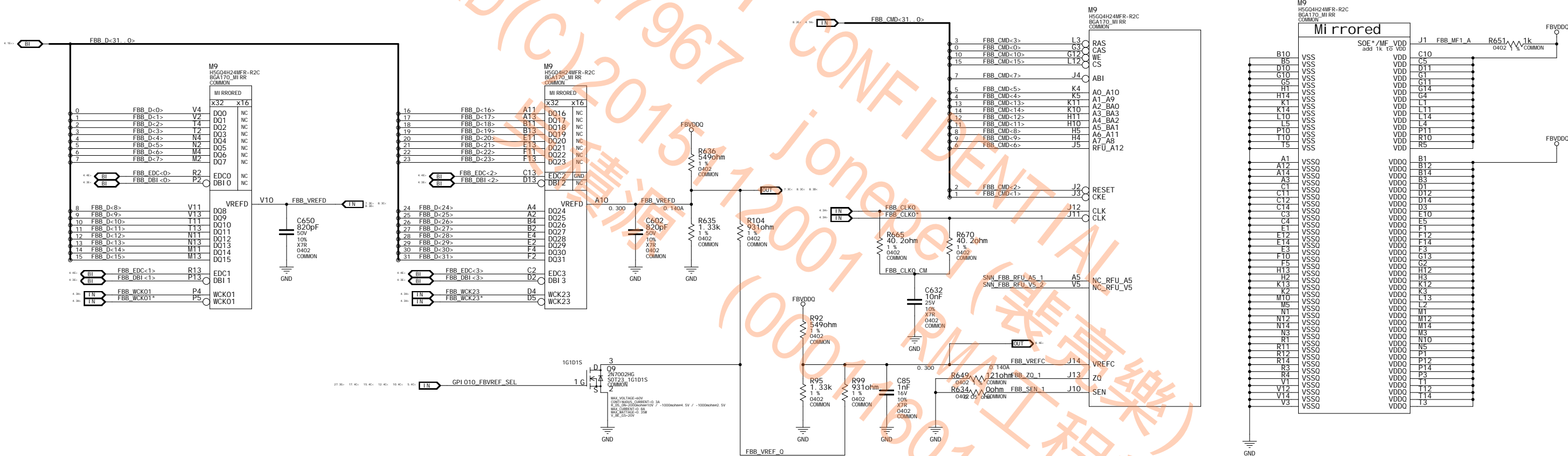
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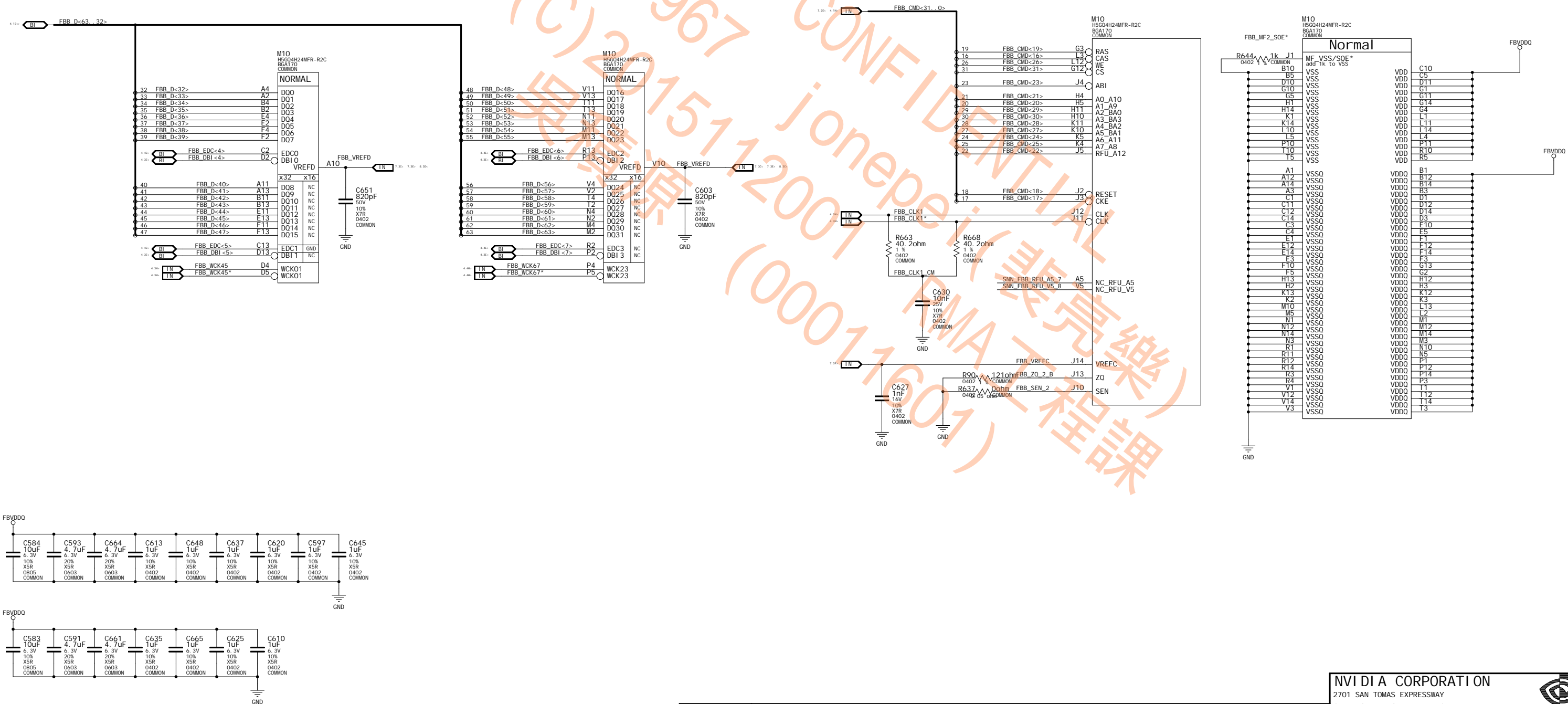


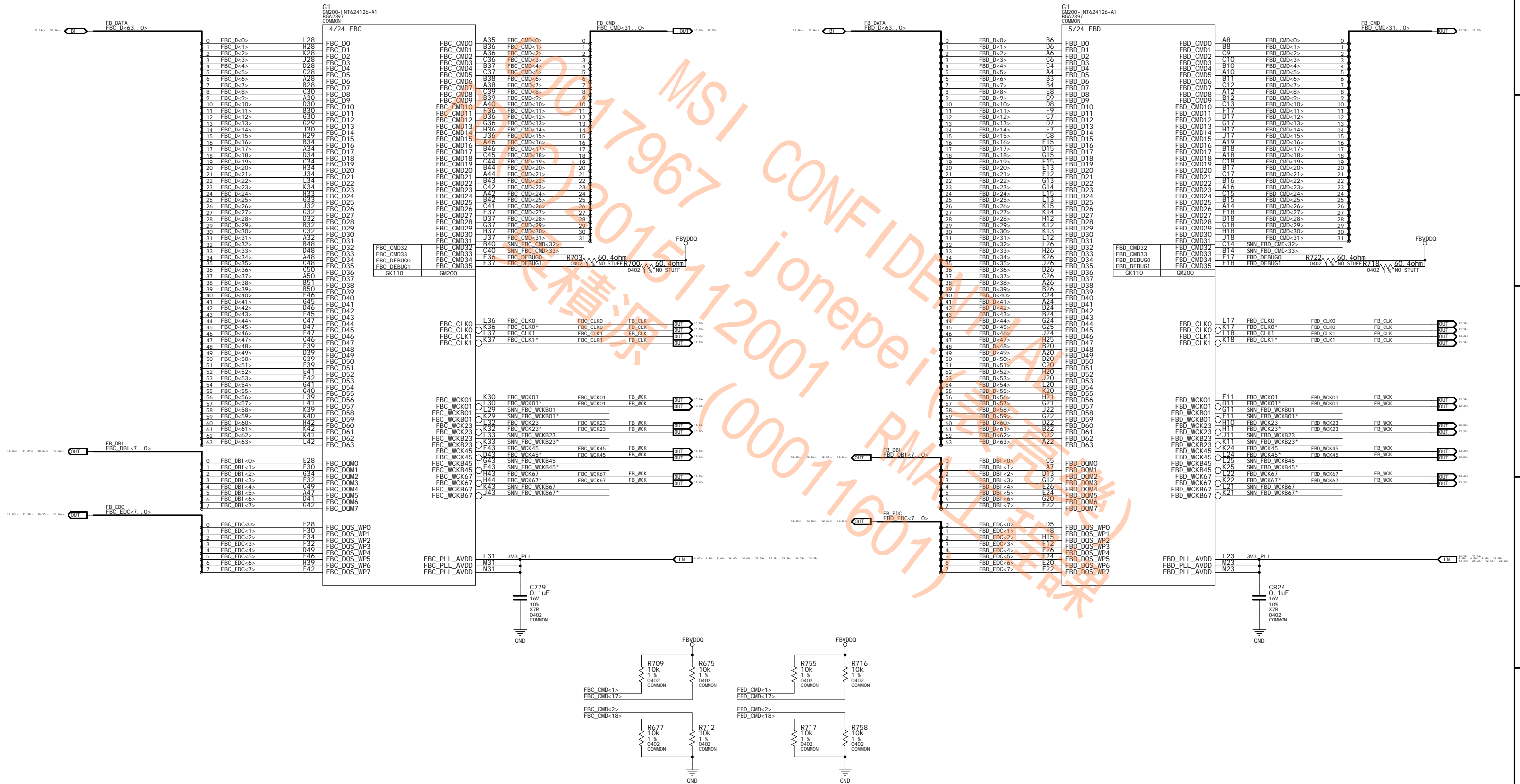


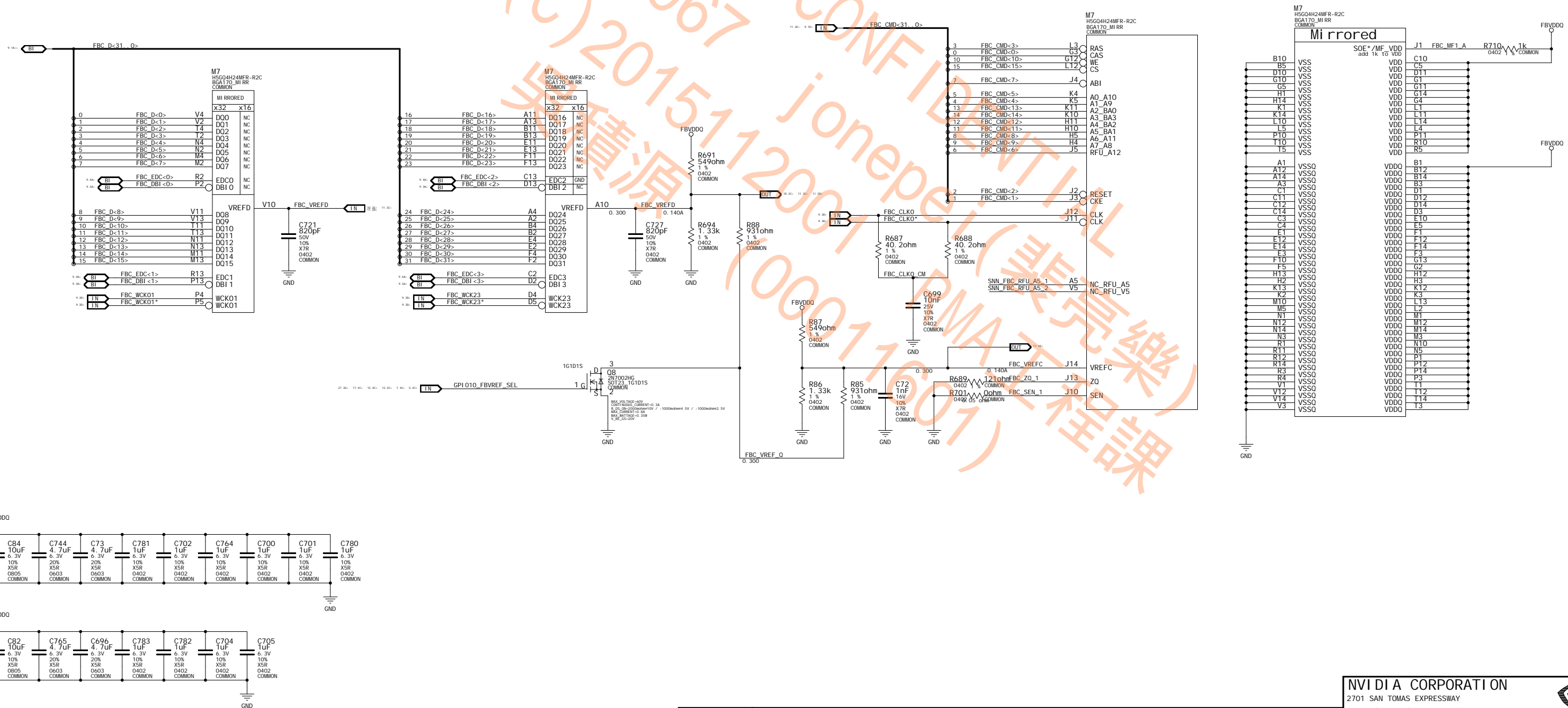
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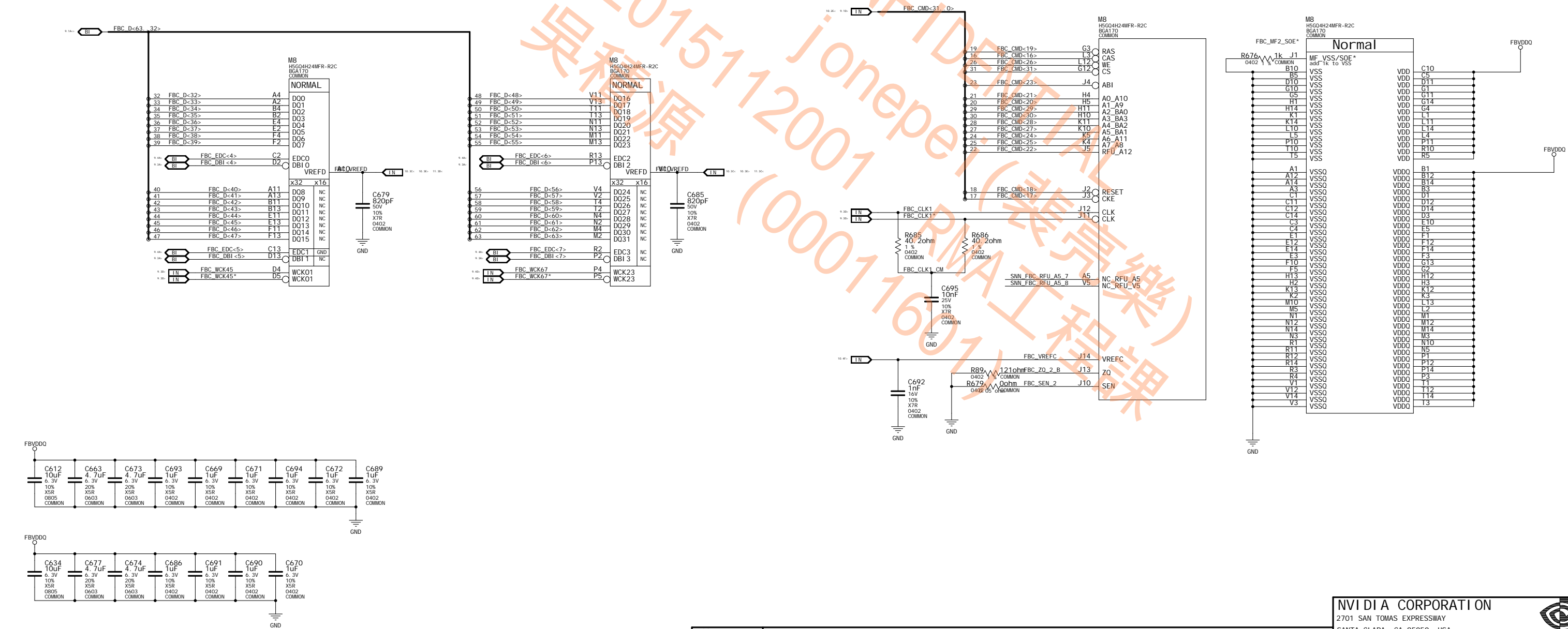












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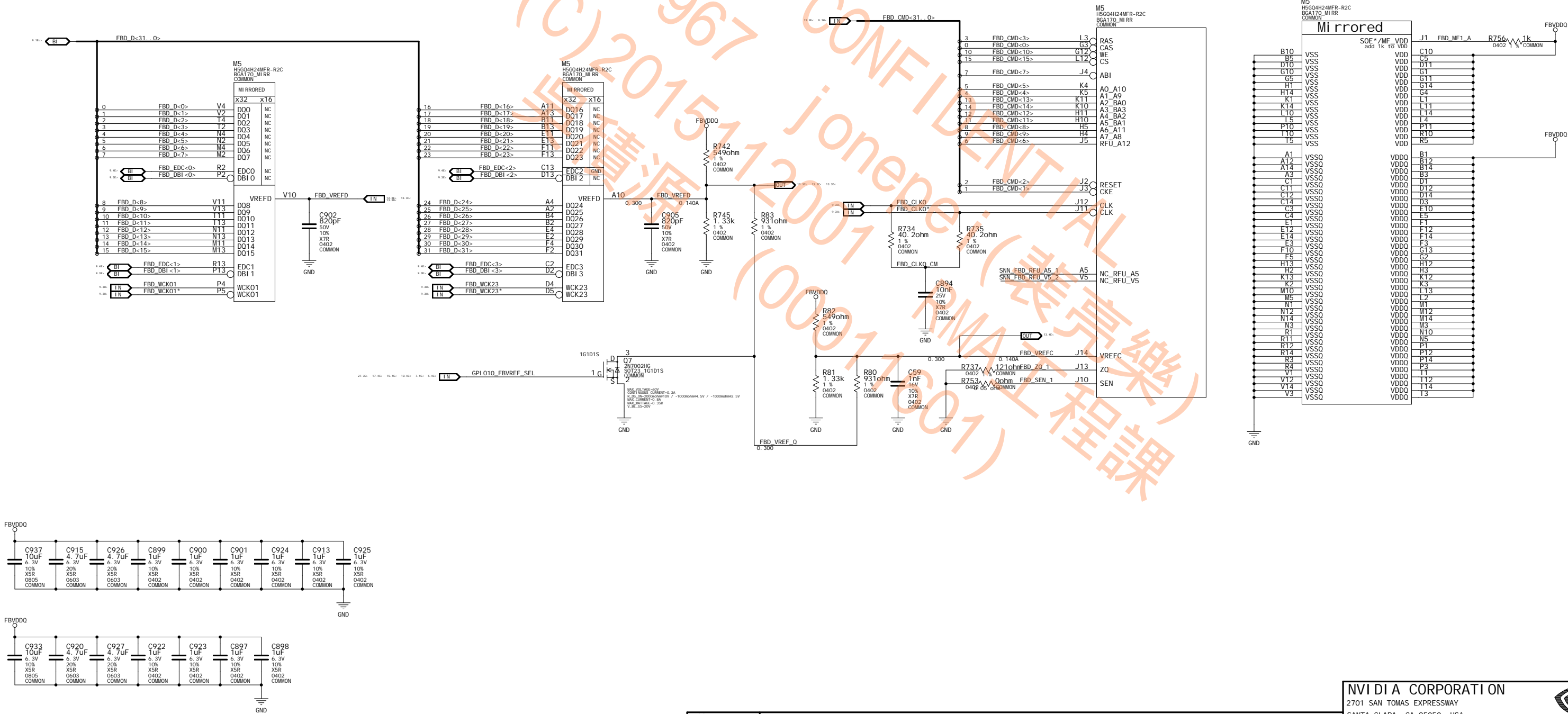
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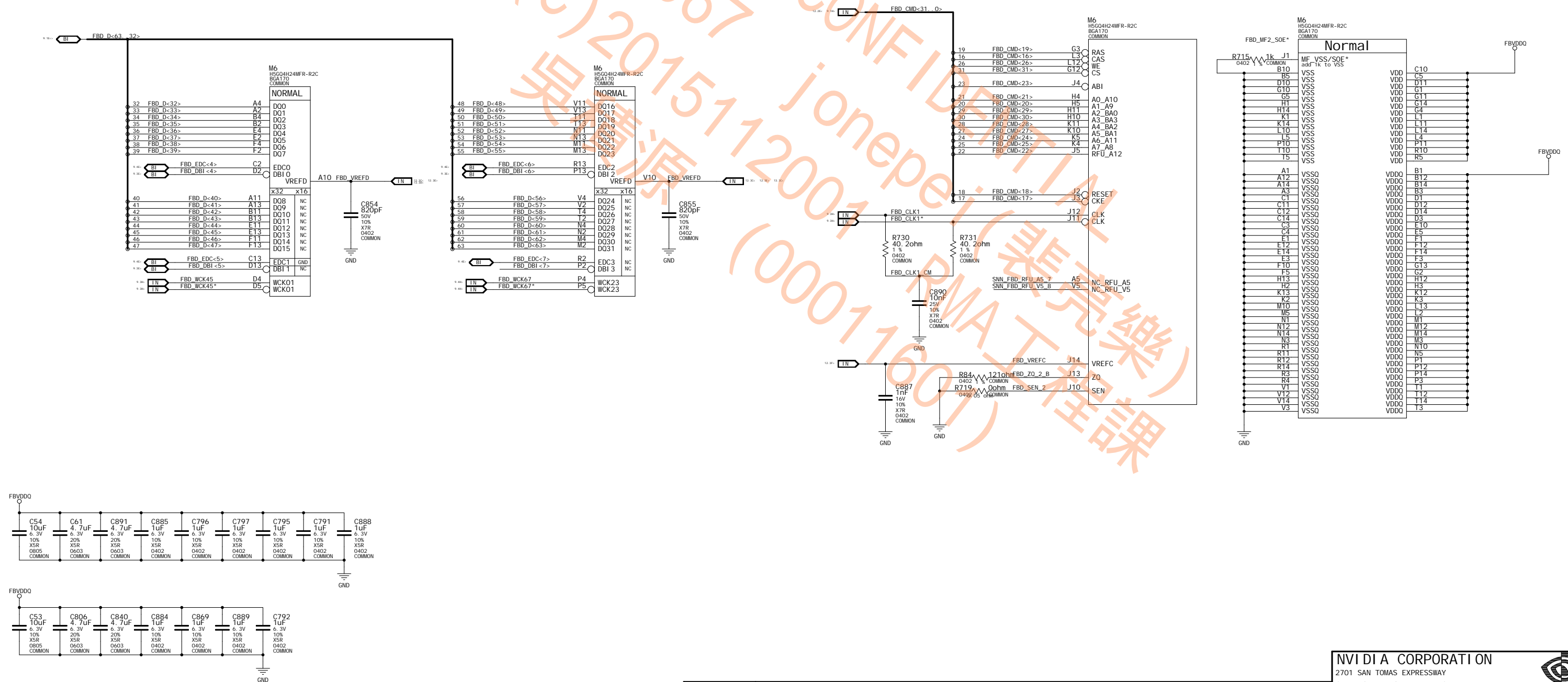
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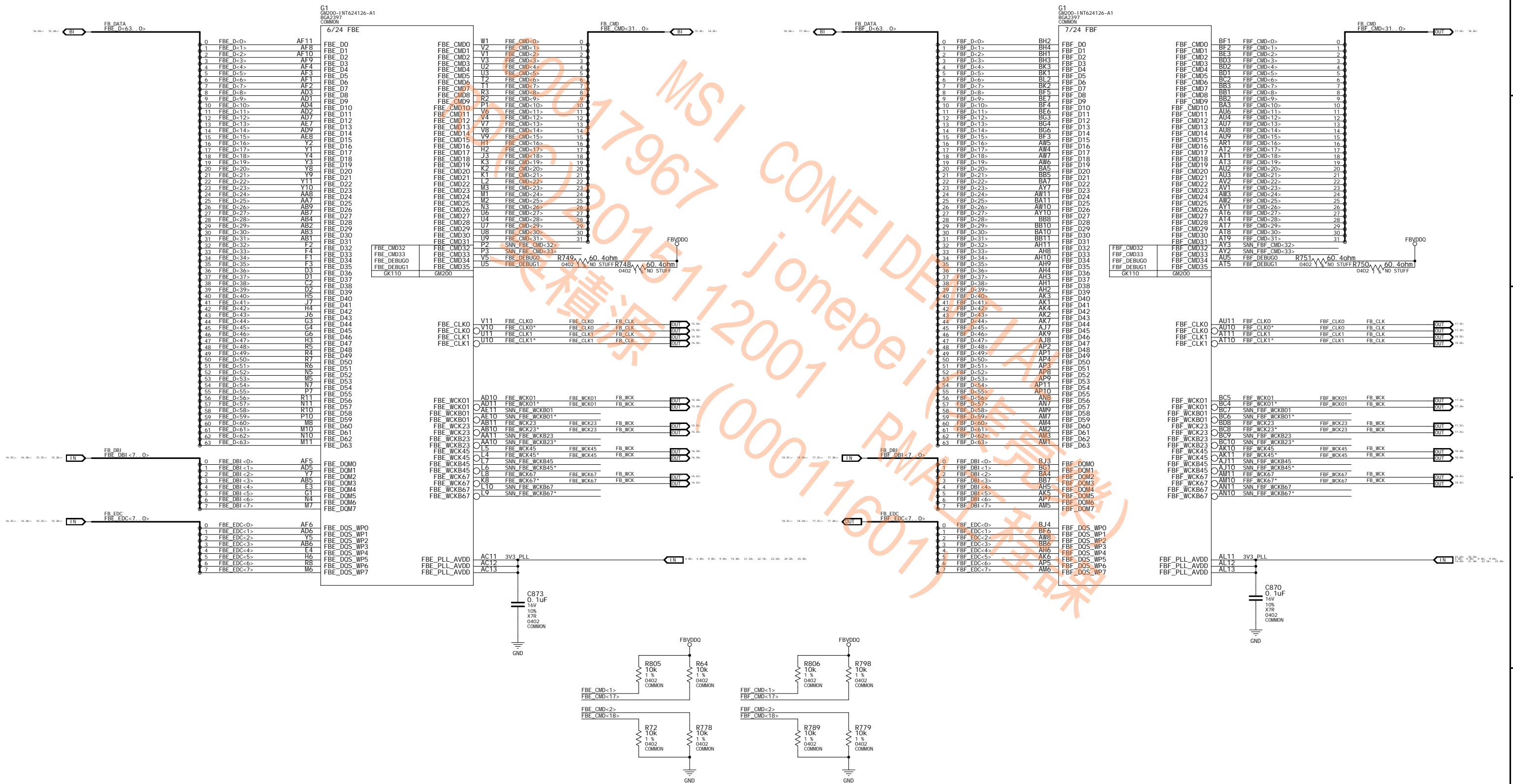
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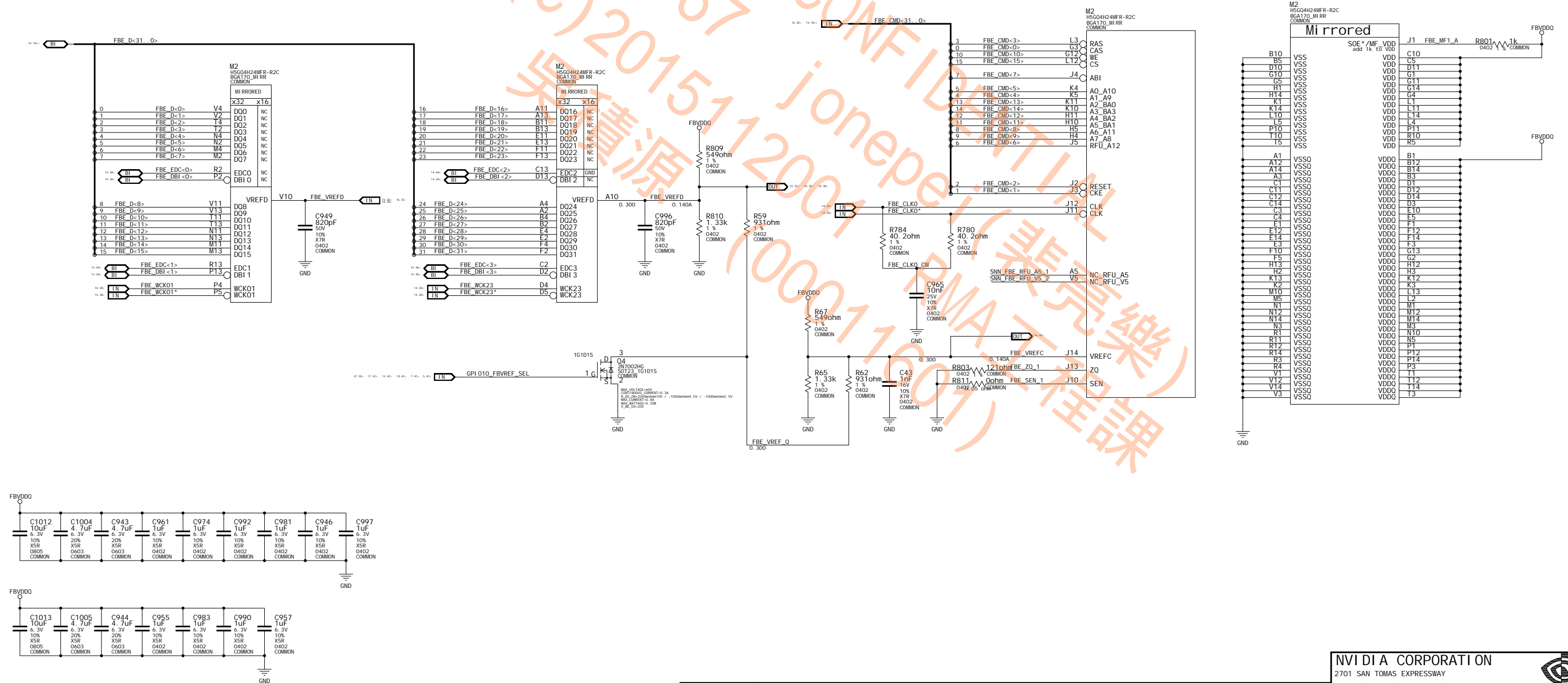


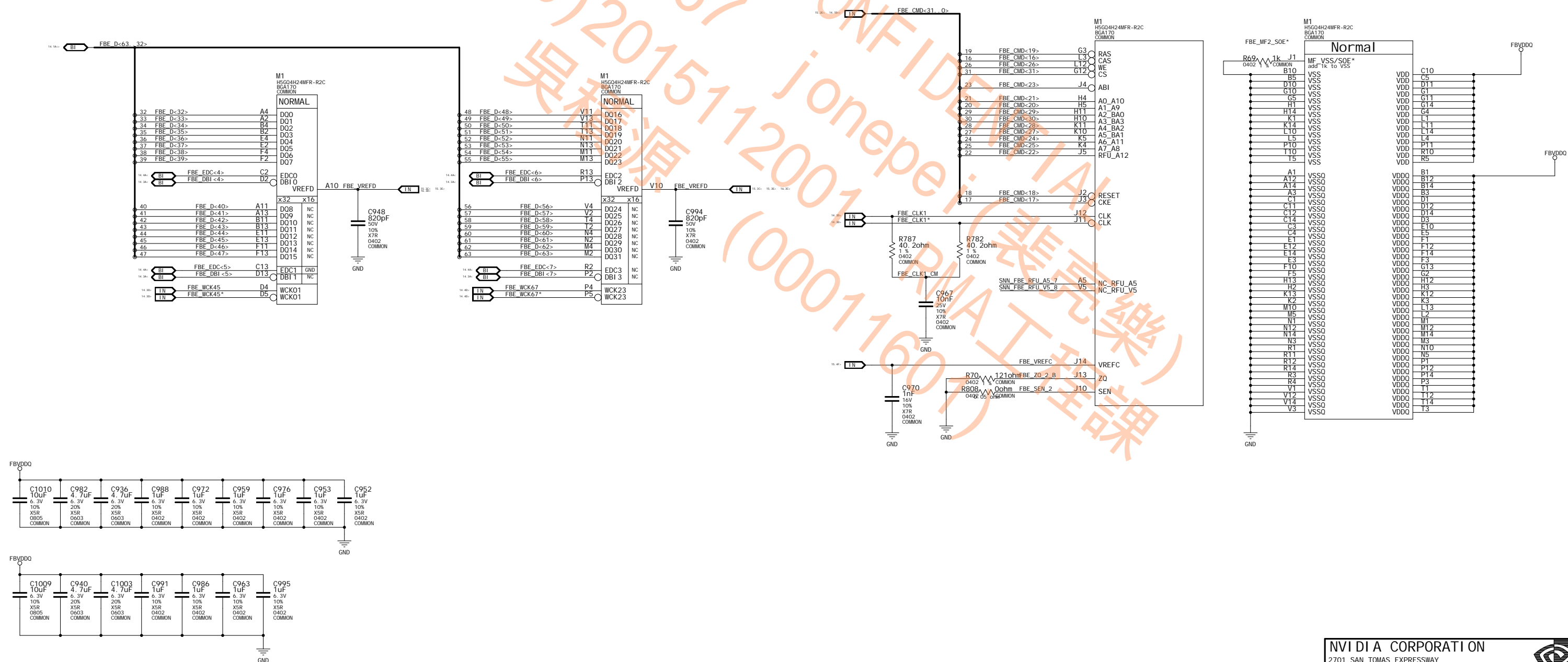
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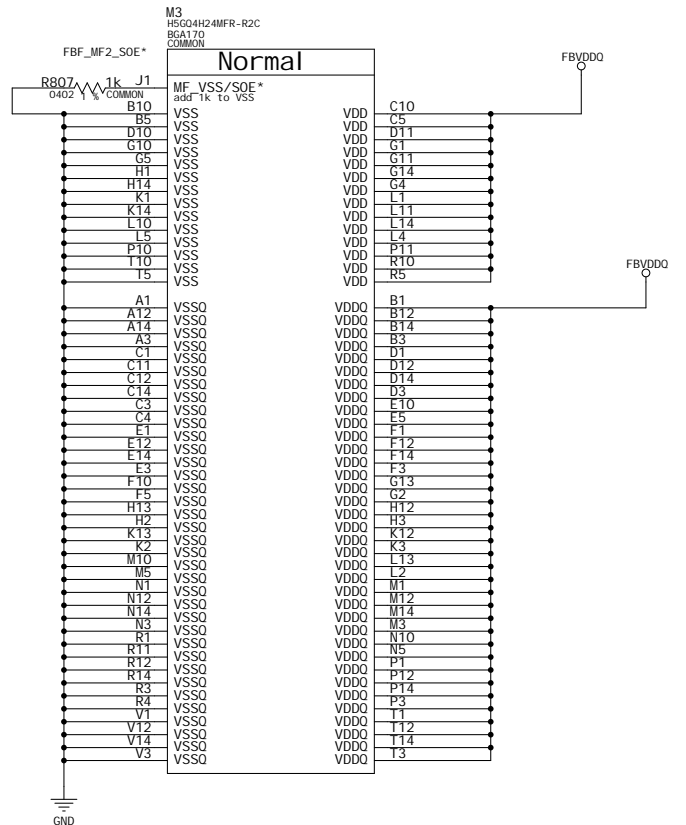


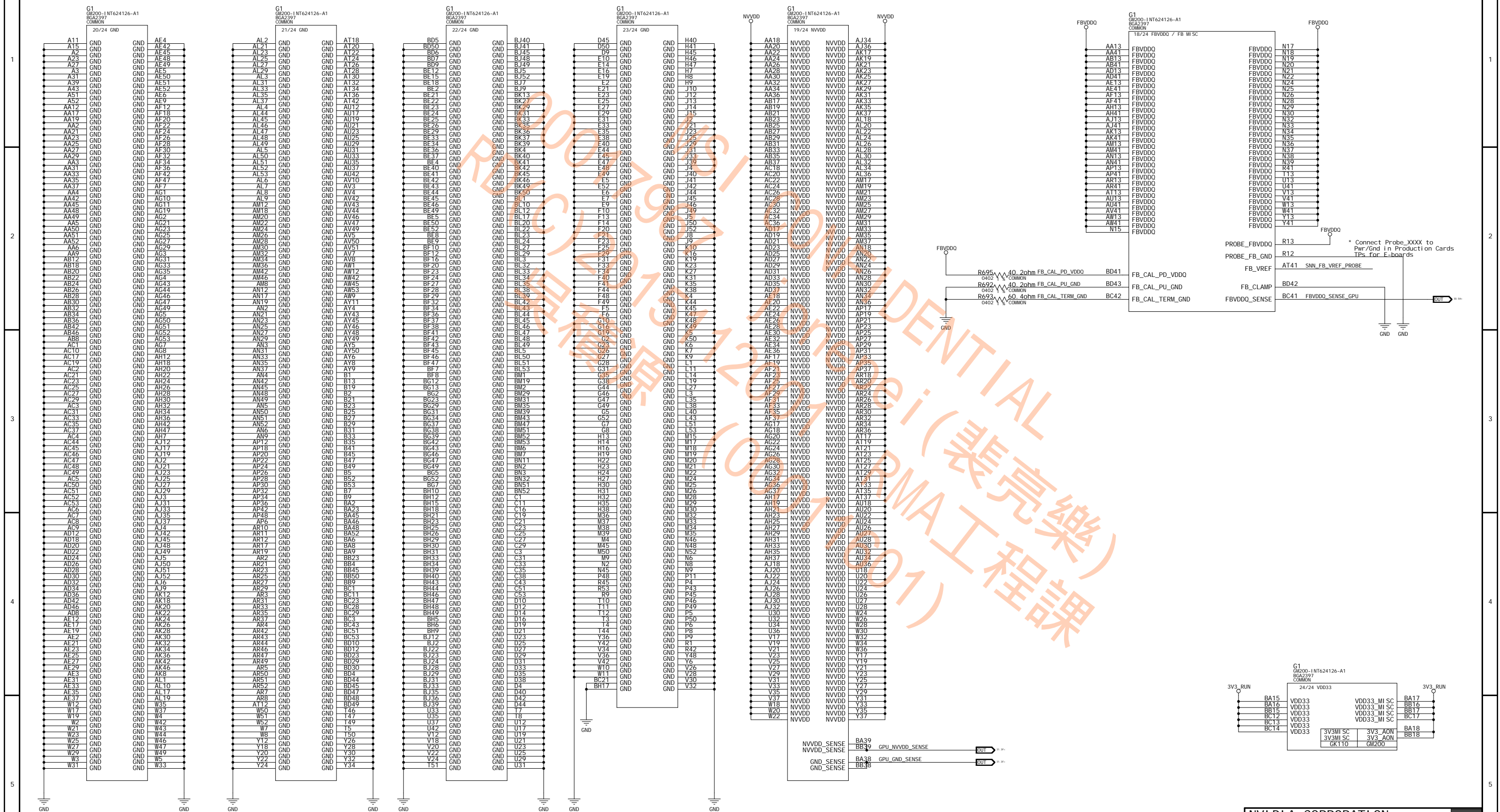


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PAGE DETAIL	MEMORY: FBE[63:32]

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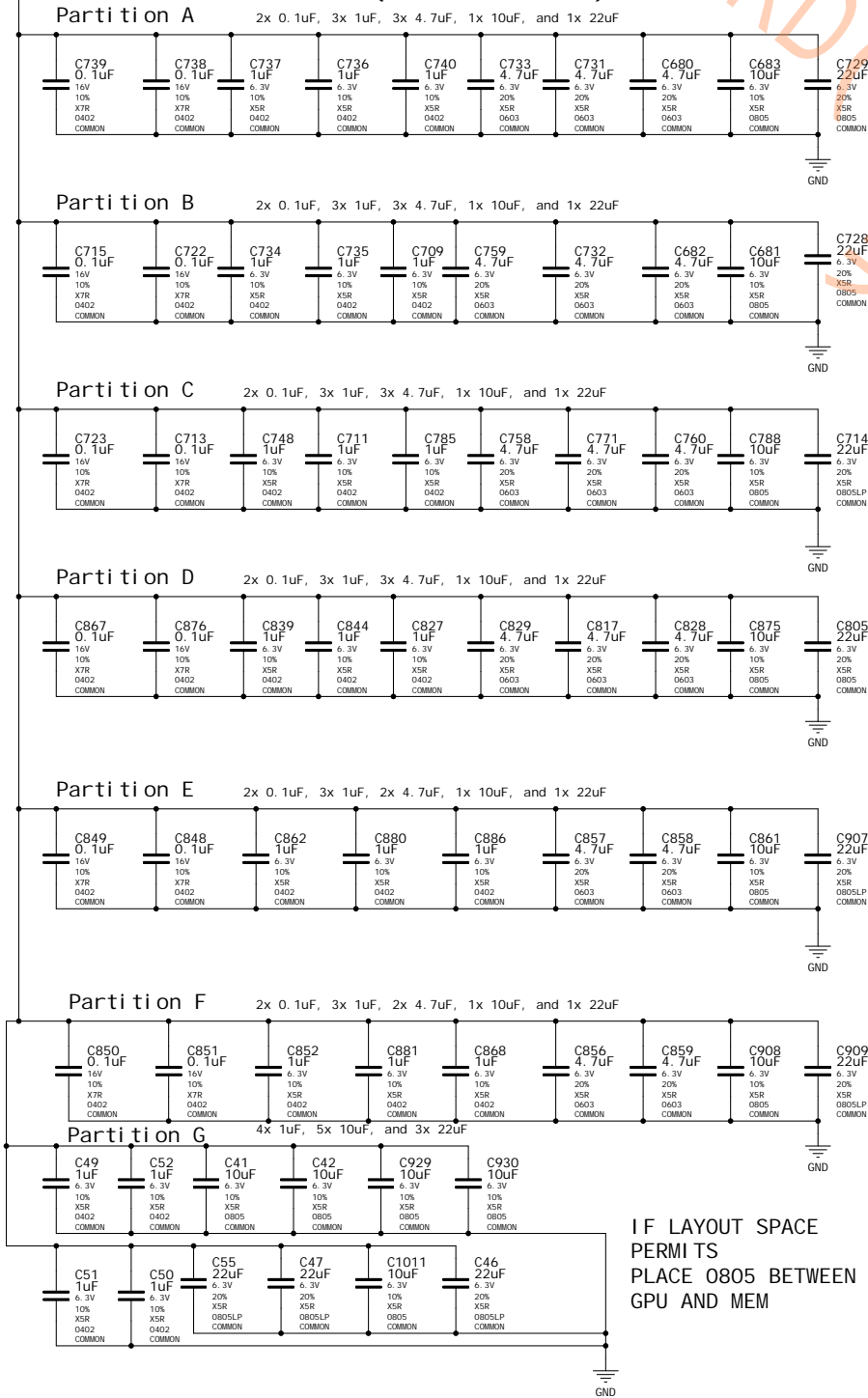
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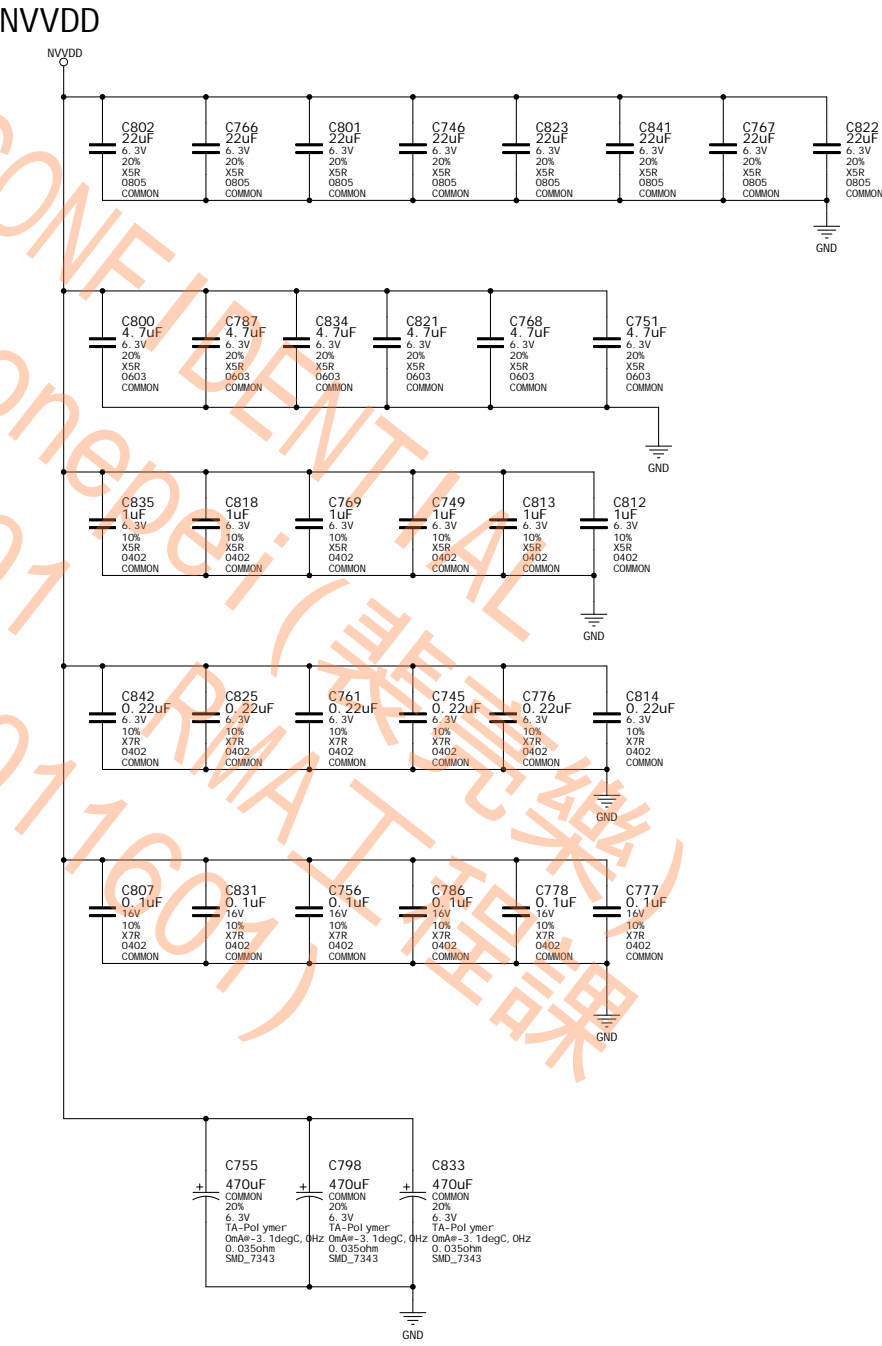
Based on GB3-X GDDR5 FBVDDQ Decap Guideline

FBVDDQ
0.1uF, 1uF, 0402 (Place Under GPU)
4.7uF, 0603 (Place Near GPU)
10uF, 0805 (Place Near GPU)
22uF, 0805 (Place Near GPU)



IF LAYOUT SPACE PERMITS
PLACE 0805 BETWEEN GPU AND MEM

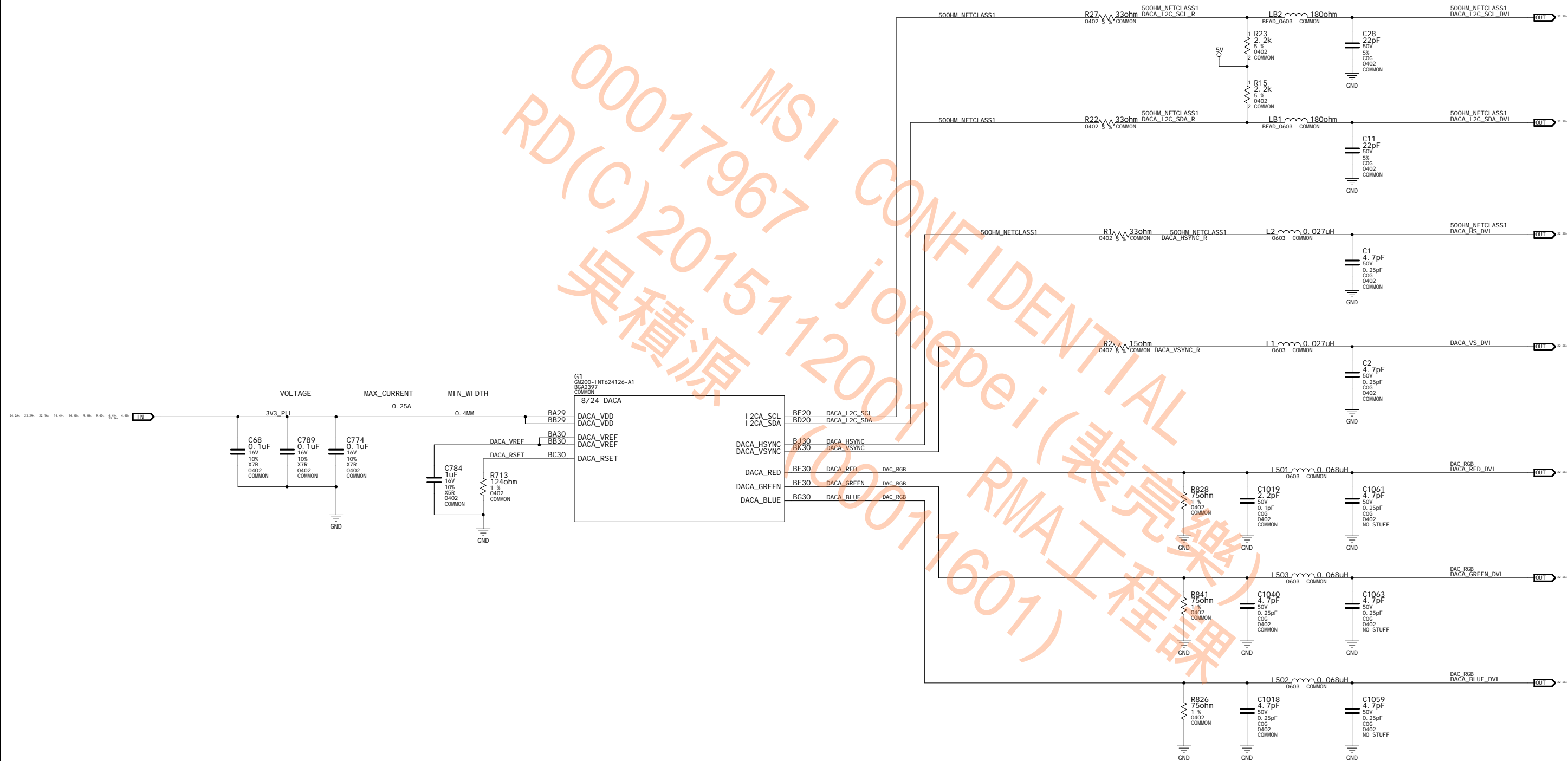
NVVDD Decoupling caps. Place under GPU.



15ci203

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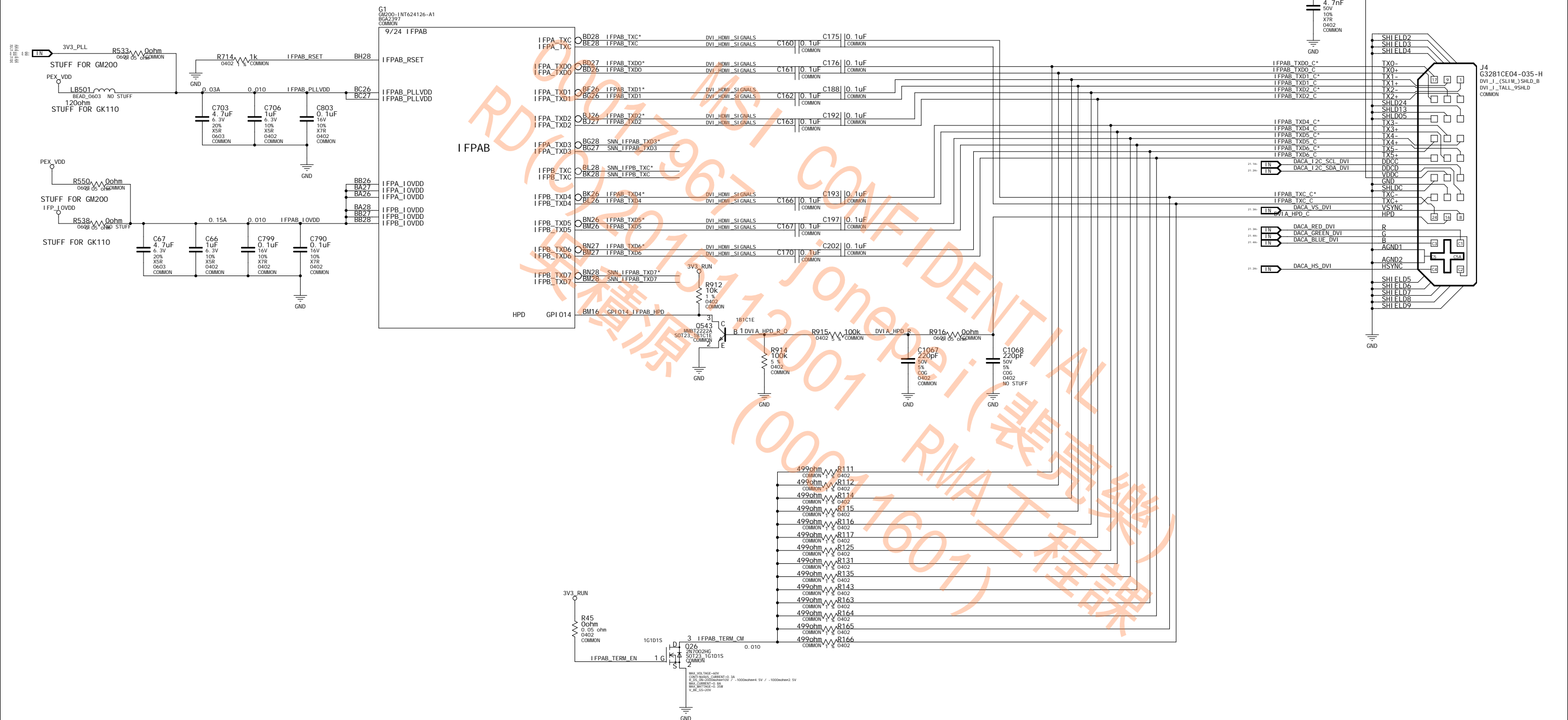


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AC COUPLING NOT NEEDED for KEPLER

REPLACE WITH ZERO OHM RESISTORS FOR KEPLER SKUs



ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DVI -
PAGE DETAIL	1FPAB DVI -I -DL

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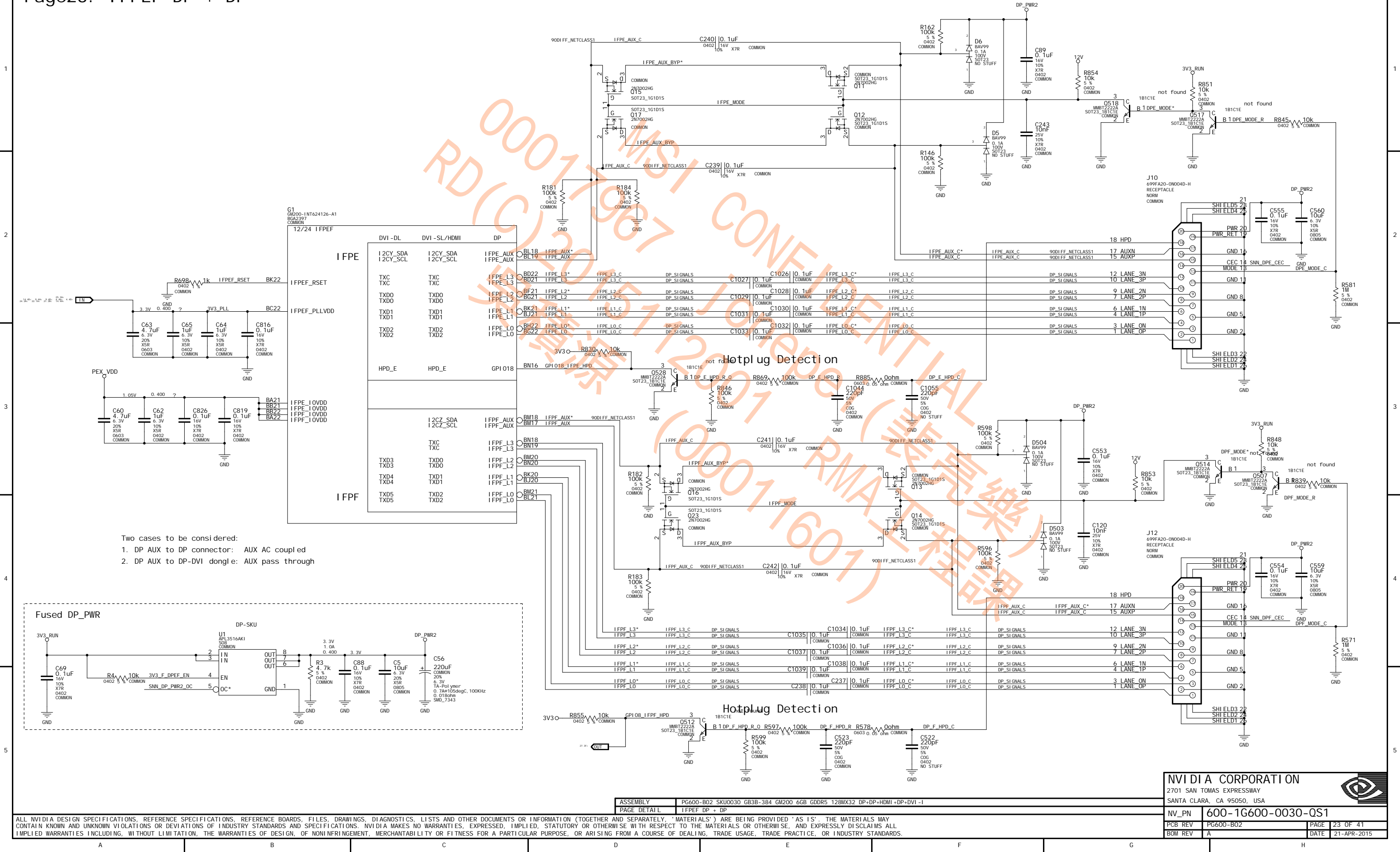
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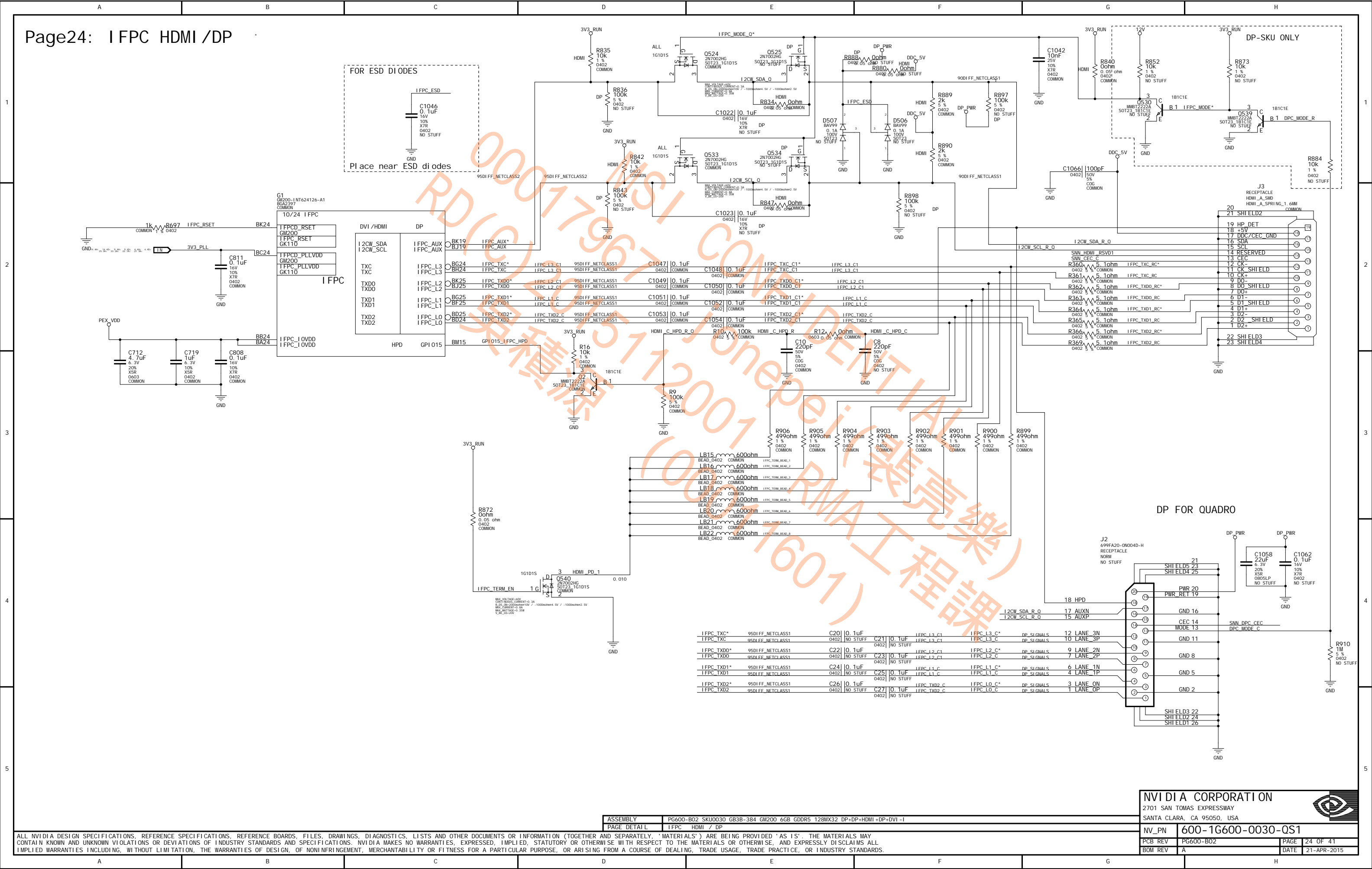
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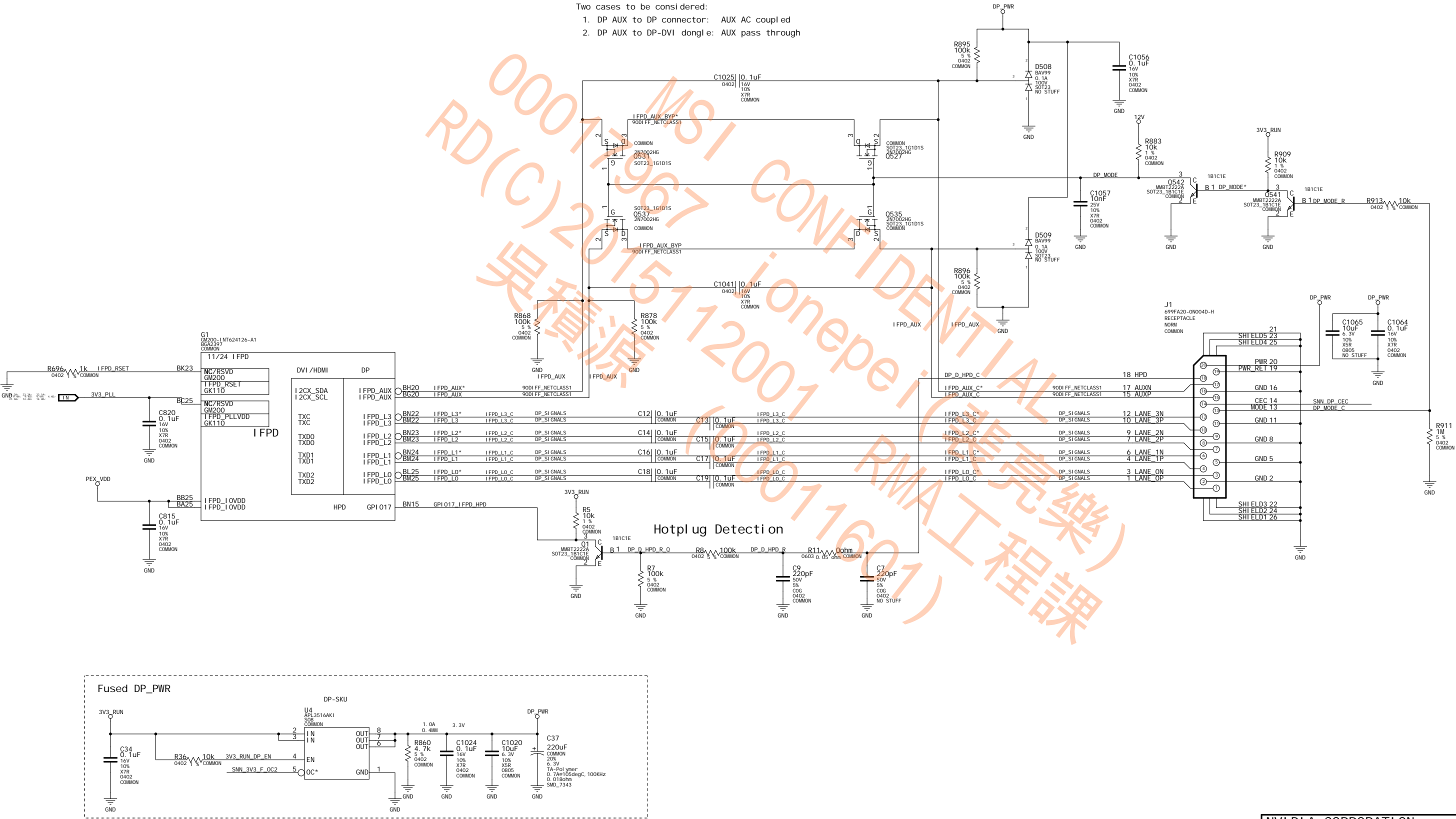
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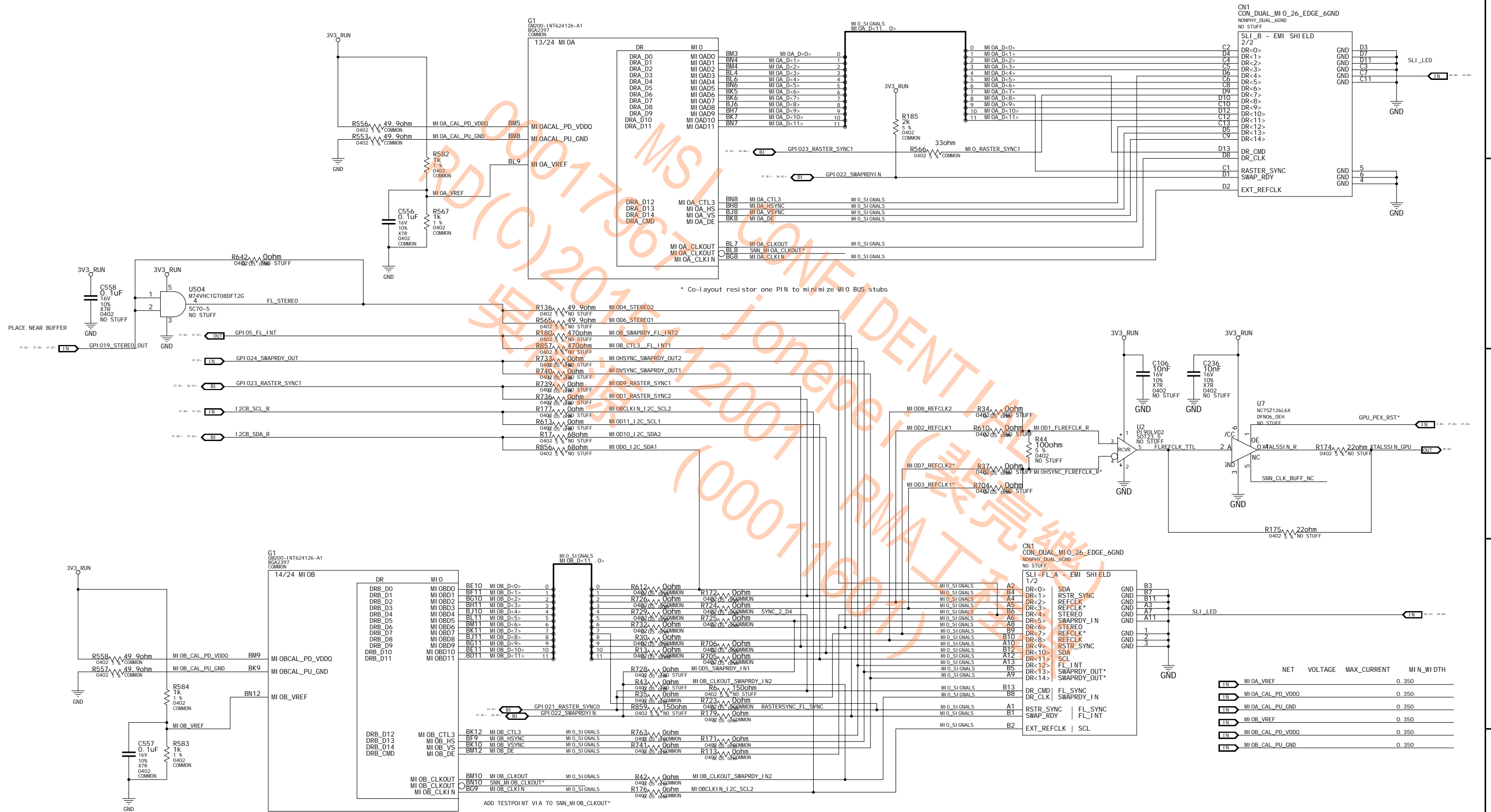
- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through









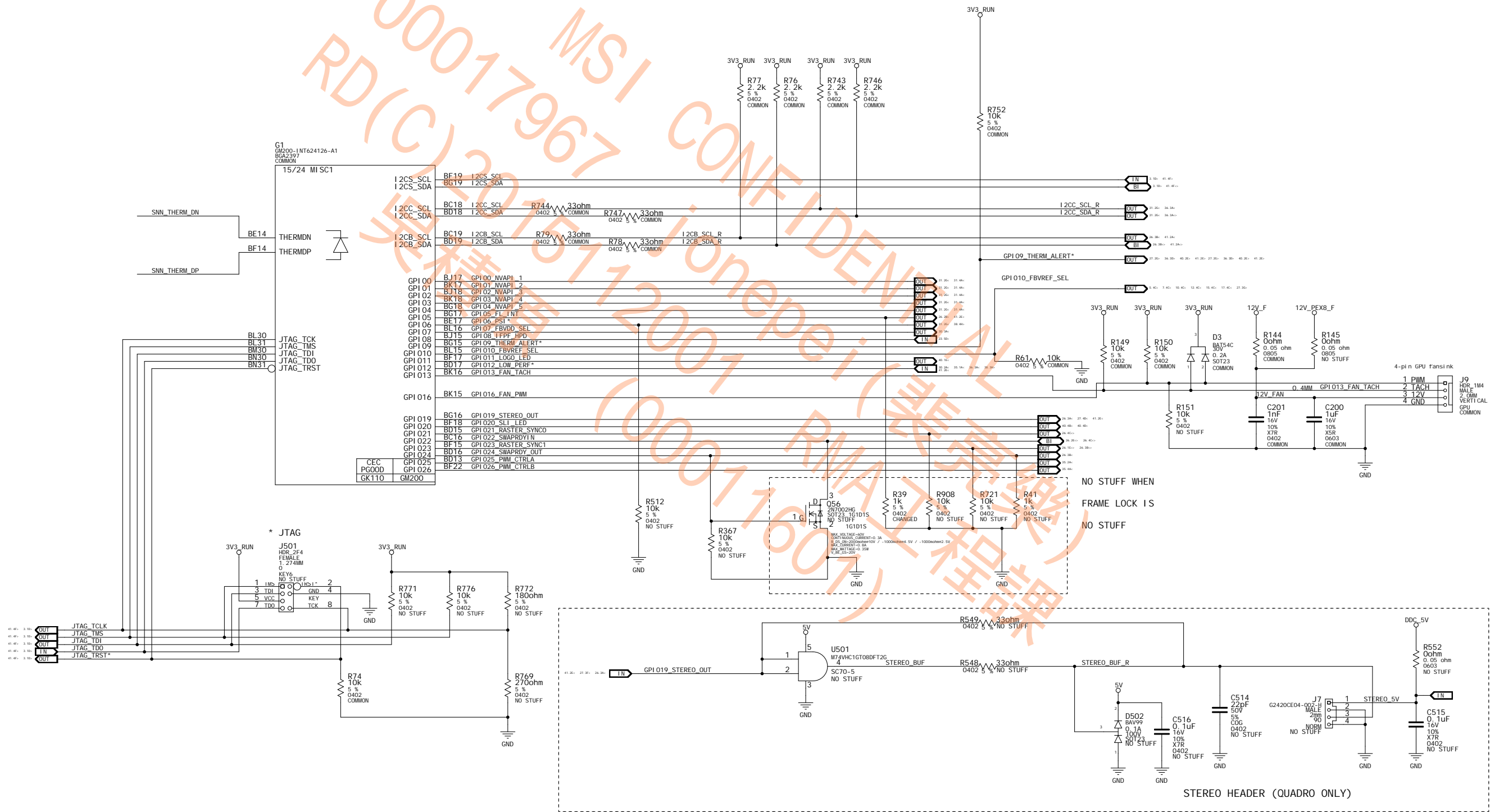
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Page26: MI 0A/B and FRAMELOCK Interface



	NET	VOLTAGE	MAX_CURRENT	MIN_WI DTH
	MI OA_VREF			0.350
	MI OA_CAL_PD_VDDQ			0.350
	MI OA_CAL_PU_GND			0.350
	MI OB_VREF			0.350
	MI OB_CAL_PD_VDDQ			0.350
	MI OB_CAL_PU_GND			0.350



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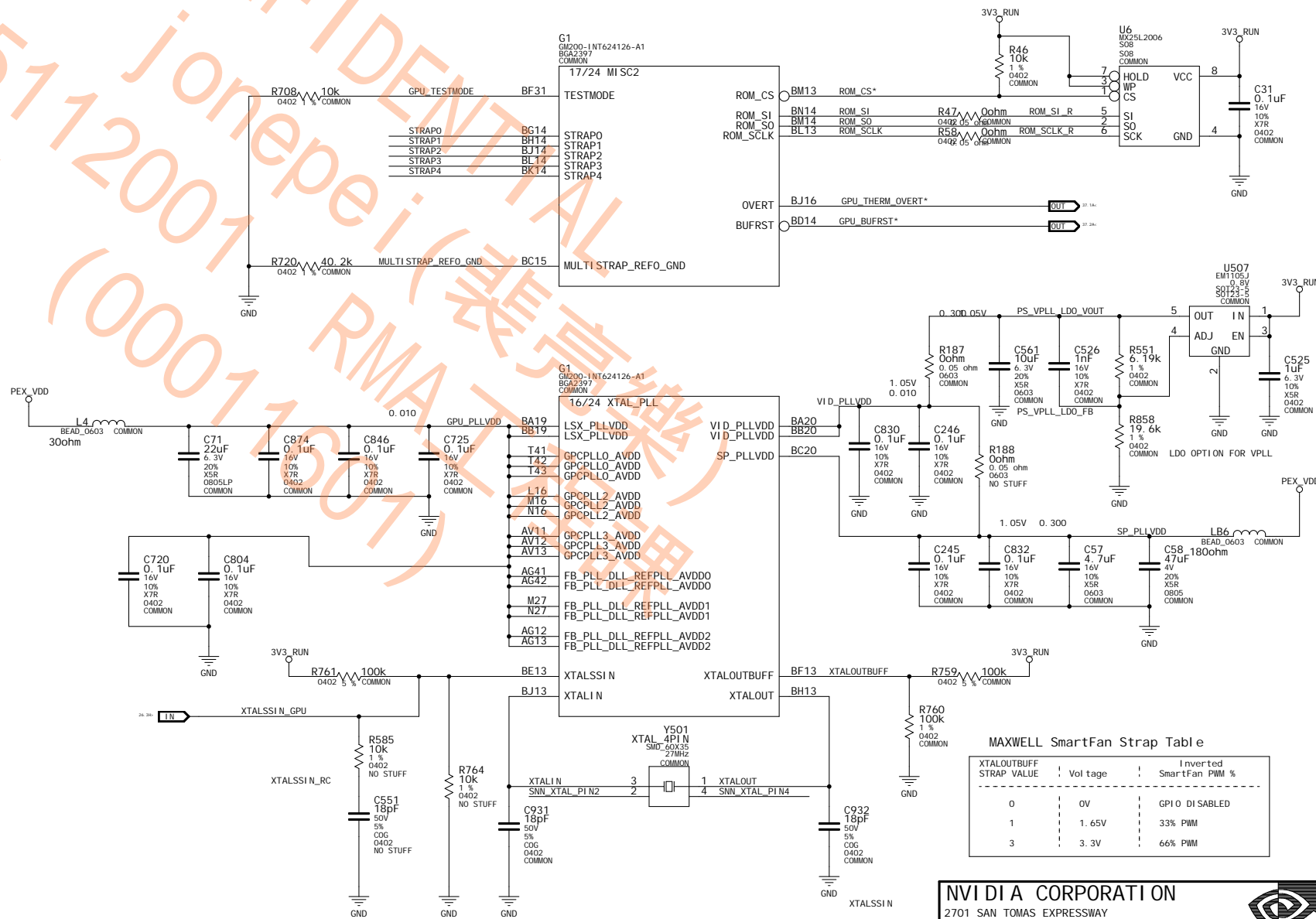
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		GK110	GM200
STRAP0	USER_BIT [3:0]*	0000*	GC6_ENABLE(3.3V) PU
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	N/A
STRAP2	PCI_DEVICEID [3:0]*	100A*	N/A
STRAP3	SOR_EXPOSED [3:0]*	1111*	N/A
STRAP4	[LSB] DP_PLL_VDD_33V*	1* FOR 3_3V*	N/A
	PEX_MAX_SPEED*	1* FOR GEN2/3*	N/A
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	N/A
	[MSB] RESERVED	0*	N/A
ROM_SI	[LSB] RAMCFG[0]*	1*	RAMCFG[0]*
	RAMCFG[1]*	0*	RAMCFG[1]*
	RAMCFG[2]*	1*	RAMCFG[2]*
	[MSB] RAMCFG[3]*	0*	RAMCFG[3]*
ROM_SO	[LSB] VGA_DEVICE*	1*	VGA_DEVICE* 1* For Enable
	SMB_ALT_ADDR*	0*	SMB_ALT_ADDR 0* For Disable
	FB[0]_APERTURE_SIZE*	1* For 128MB*	PCI_E_CFG 0* For Desktop
	[MSB] FB[1]_APERTURE_SIZE*	0* For 128MB*	DEVICE_SEL 0* For Device A
ROM_SCLK	[LSB] PEX_PLL_EN_TERM100*	0* DISABLED*	SOR0_EXPOSED
	PCI_DEVICEID_EXT[5]*	0*	SOR1_EXPOSED
	SUB_VENDOR*	1* Dedicated BIOS*	SOR2_EXPOSED
	[MSB] PCI_DEVICEID_EXT[4]*	0*	SOR3_EXPOSED


	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

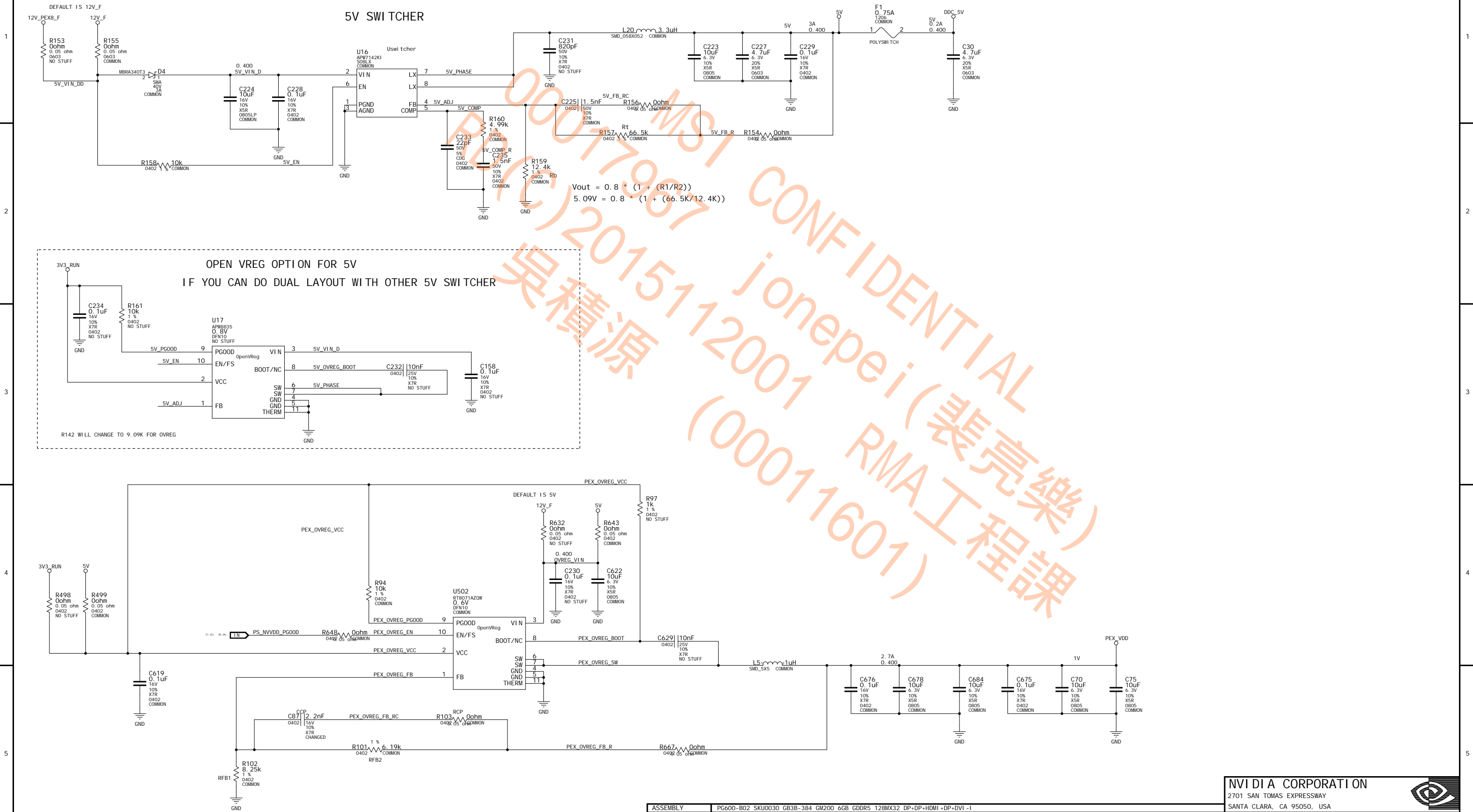
x32 DENSITY MODE STRAPS			
CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	128Mx32	384-bi t	El pi da
0010	128Mx32	384-bi t	Hyni x
0011	128Mx32	384-bi t	Samsung
0100	64Mx32	384-bi t	Hyni x B
0101	64Mx32	384-bi t	El pi da
0110	64Mx32	384-bi t	Hyni x
0111	64Mx32	384-bi t	Samsung
1000	Reserved		
1001	128Mx32	320-bi t	El pi da
1010	128Mx32	320-bi t	Hyni x
1011	128Mx32	320-bi t	Samsung
1100	64Mx32	320-bi t	Hyni x B
1101	64Mx32	320-bi t	El pi da
1110	64Mx32	320-bi t	Hyni x
1111	64Mx32	320-bi t	Samsung

x16 DENSITY MODE STRAPS			
CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	256Mx16	384-bi t	El pi da
0010	256Mx16	384-bi t	Hyni x
0011	256Mx16	384-bi t	Samsung
0100	128Mx16	384-bi t	Hyni x B
0101	128Mx16	384-bi t	El pi da
0110	128Mx16	384-bi t	Hyni x
0111	128Mx16	384-bi t	Samsung
1000	Reserved		
1001	256Mx16	320-bi t	El pi da
1010	256Mx16	320-bi t	Hyni x
1011	256Mx16	320-bi t	Samsung
1100	128Mx16	320-bi t	Hyni x B
1101	128Mx16	320-bi t	El pi da
1110	128Mx16	320-bi t	Hyni x
1111	128Mx16	320-bi t	Samsung



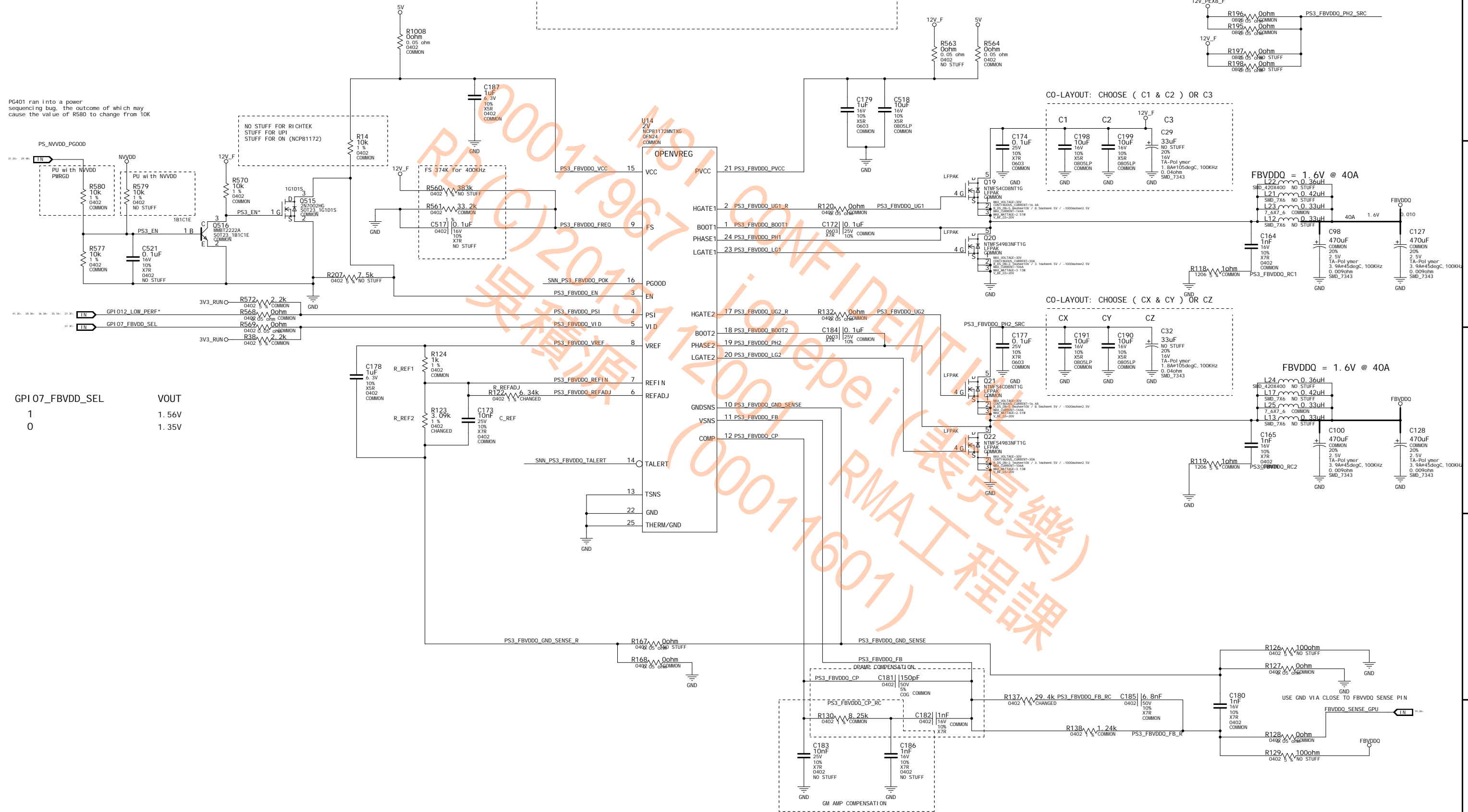
MAXWELL SmartFan Strap Table		
XTALOUTBUFF STRAP VALUE	Vol tage	Inverted SmartFan PWM %
0	0V	GPIO 0 DISABLED
1	1.65V	33% PWM
3	3.3V	66% PWM

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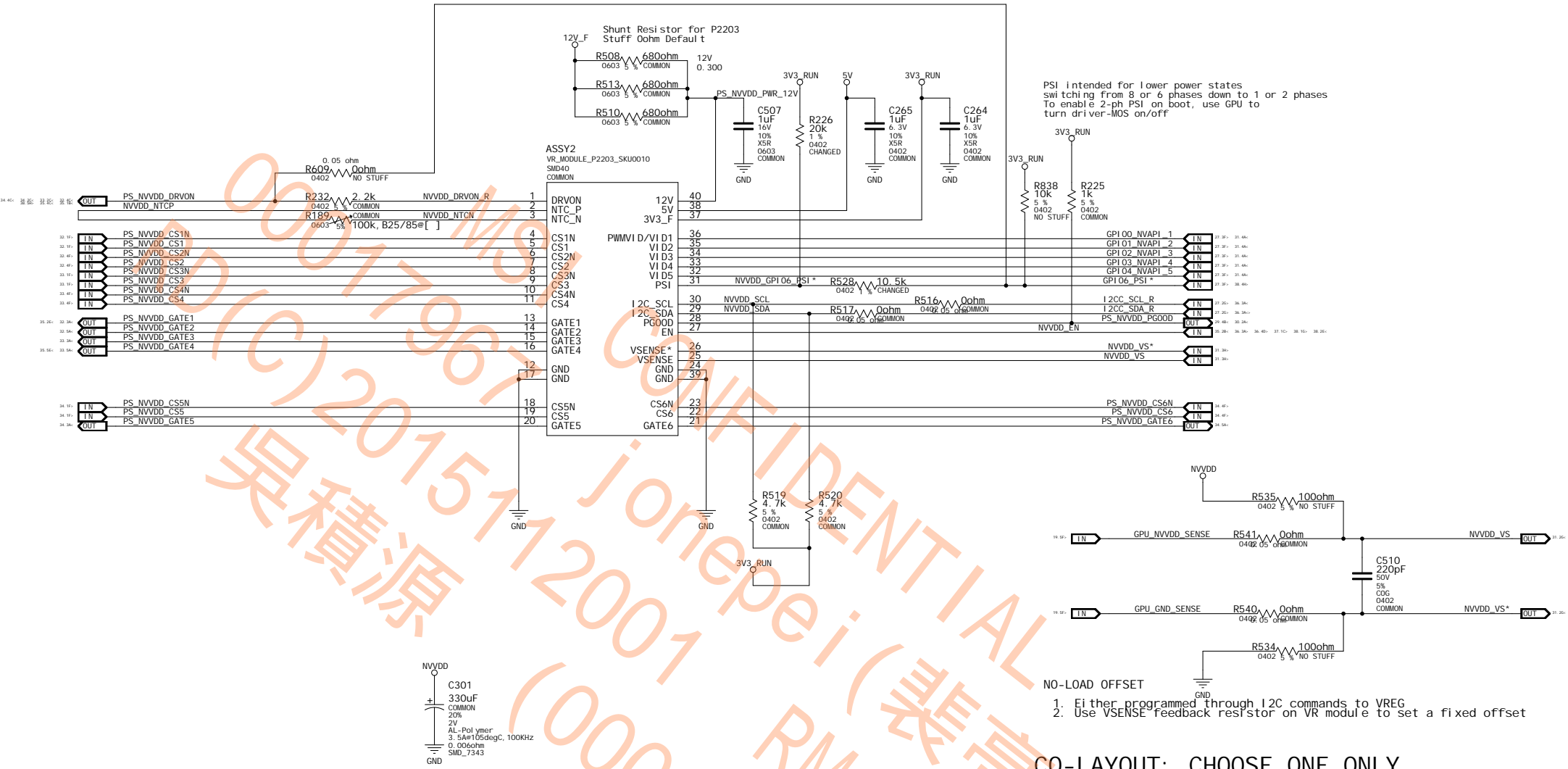


$$V_{out} = 0.8 * (1 + (R1/R2))$$
$$5.09V = 0.8 * (1 + (66.5K/12.4K))$$

OPEN VREG OPTION FOR 5V
IF YOU CAN DO DUAL LAYOUT WITH OTHER 5V SWITChER

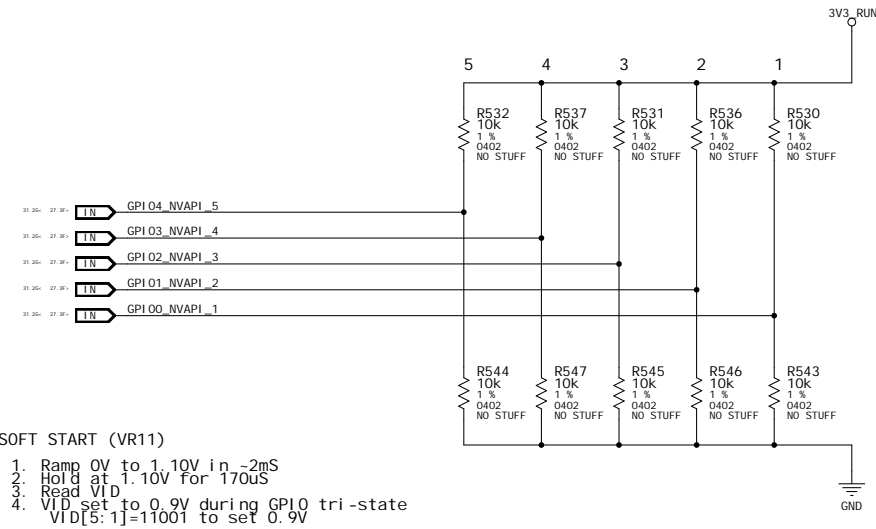


VID Table					
GPI_O4	GPI_O3	GPI_O2	GPI_O1	GPI_O0	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



- NO-LOAD OFFSET
1. Either programmed through I2C commands to VREG
 2. Use VSENSE feedback resistor on VR module to set a fixed offset

CO-LAYOUT: CHOOSE ONE ONLY



- SOFT START (VR11)
1. Ramp 0V to 1.10V in ~2ms
 2. Hold at 1.10V for 170us
 3. Read VID
 4. VID set to 0.9V during GPI0 tri-state
- VID[5:1]=11001 to set 0.9V

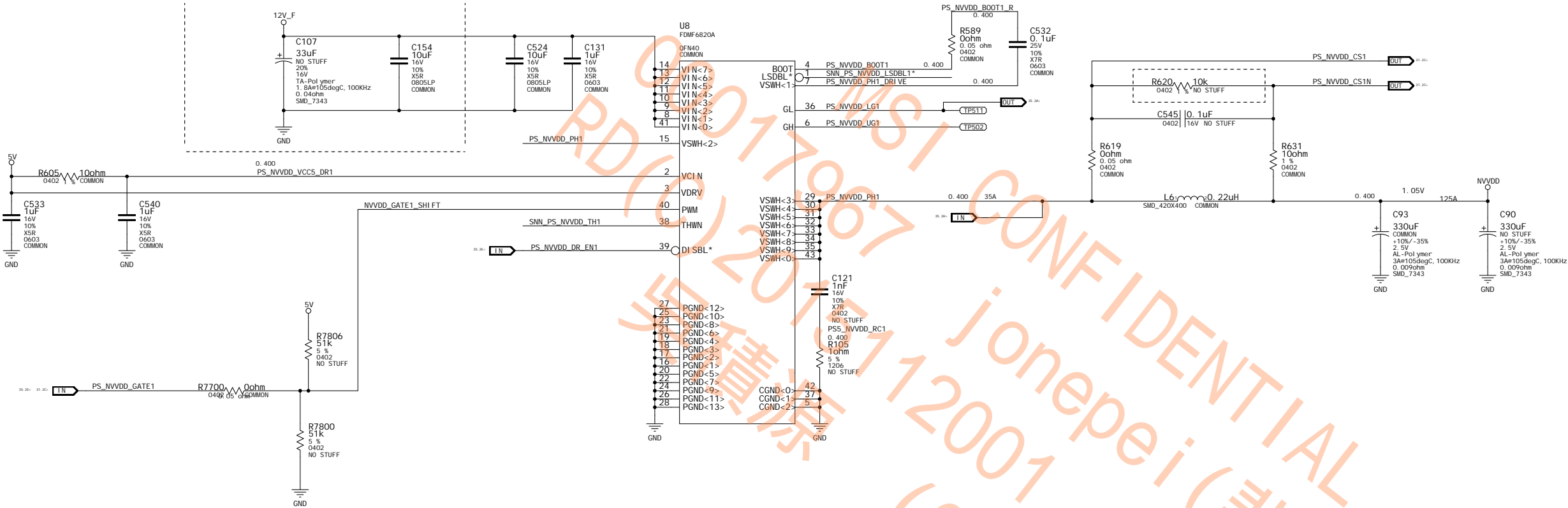
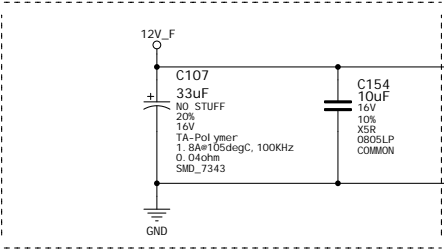
- P-STATE VOLTAGES
1. P0 at 1.05V to 1.15V (depending on VB)
 2. P8/P12 at 0.80V

ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI+DP+DVI-I
PAGE DETAIL	PS: NVVDD Controller

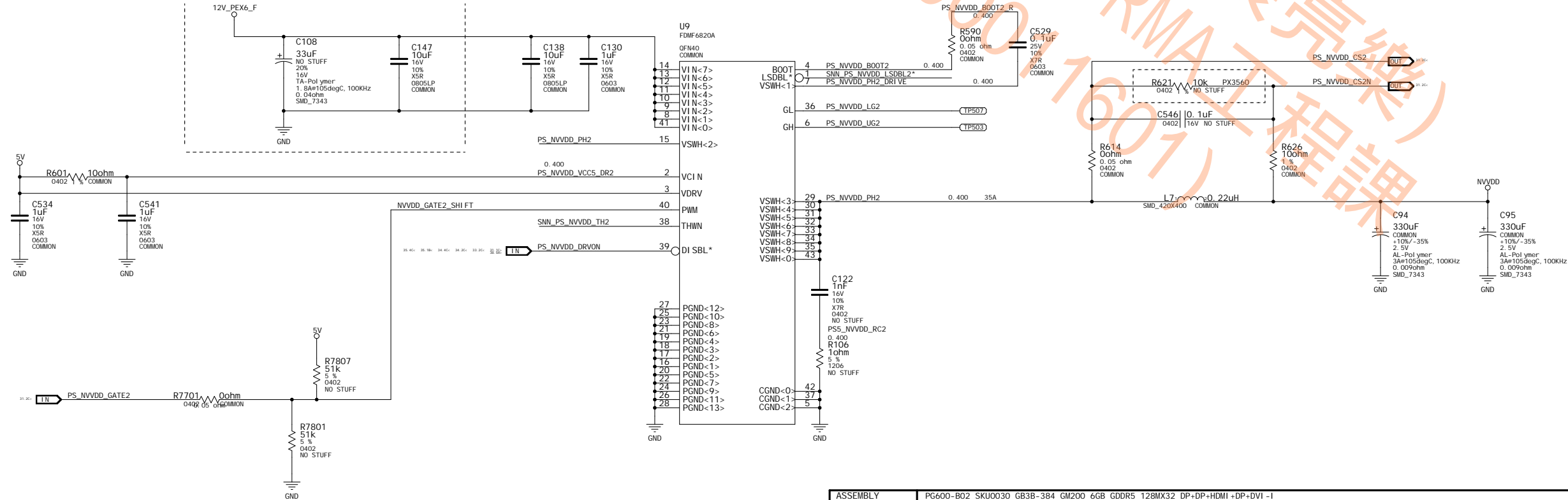
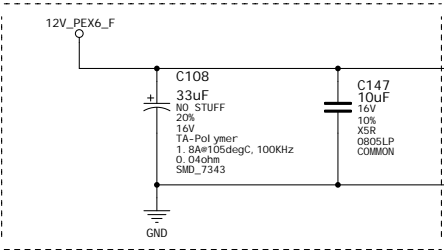
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CO-LAYOUT: STUFF ONLY ONE



CO-LAYOUT: STUFF ONLY ONE



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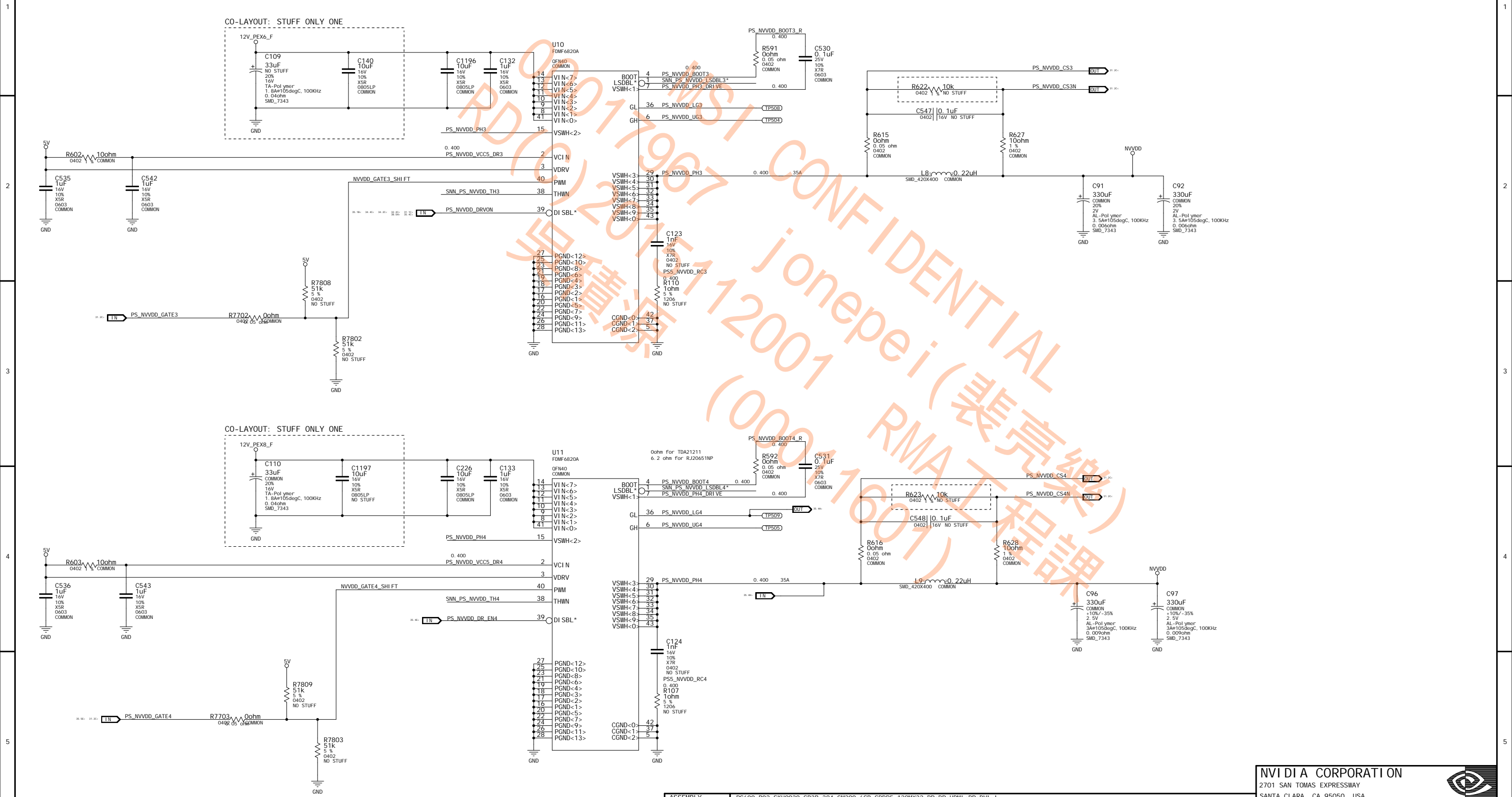
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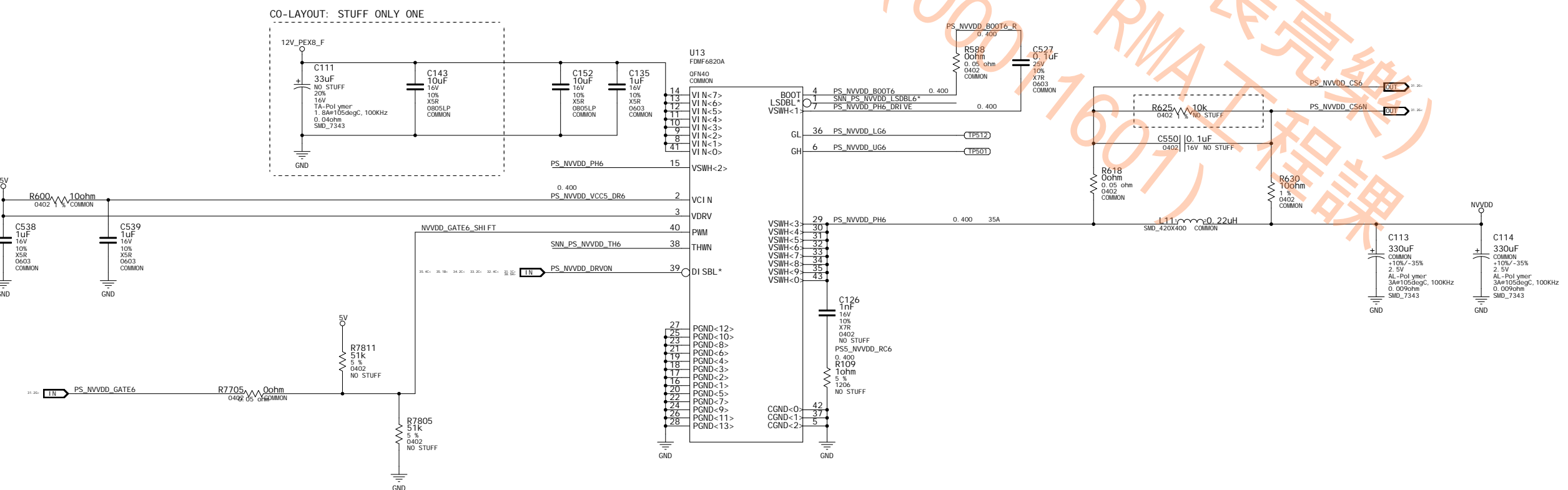
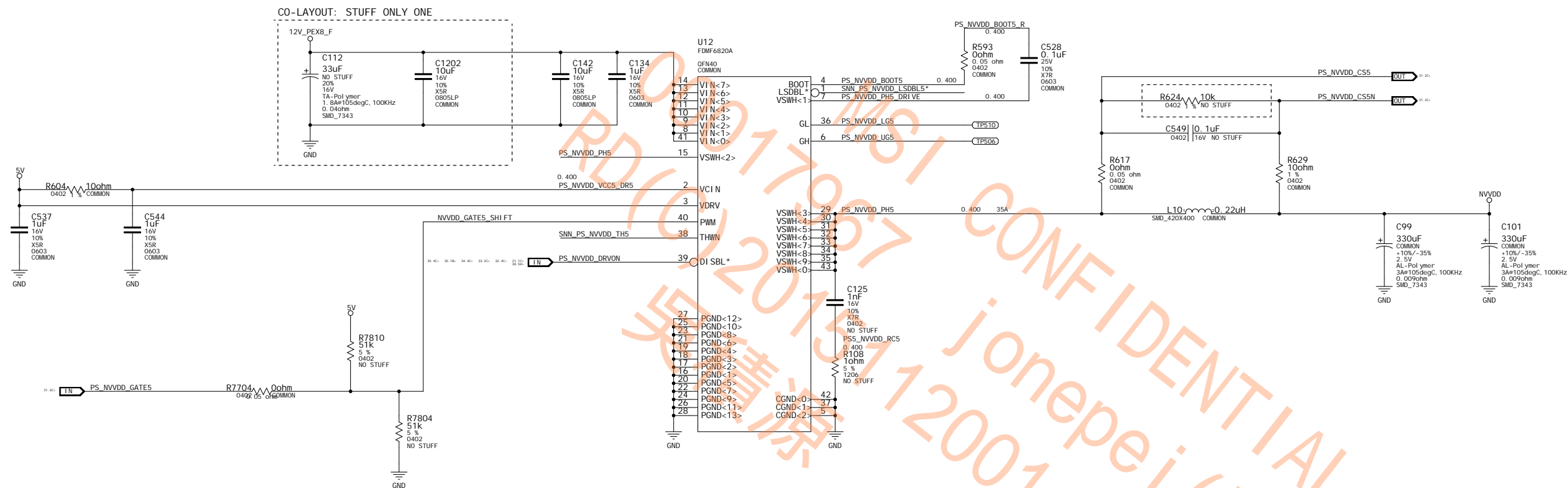


ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DVI-I
PAGE DETAIL	PS: NVVDD Phase 1, 2

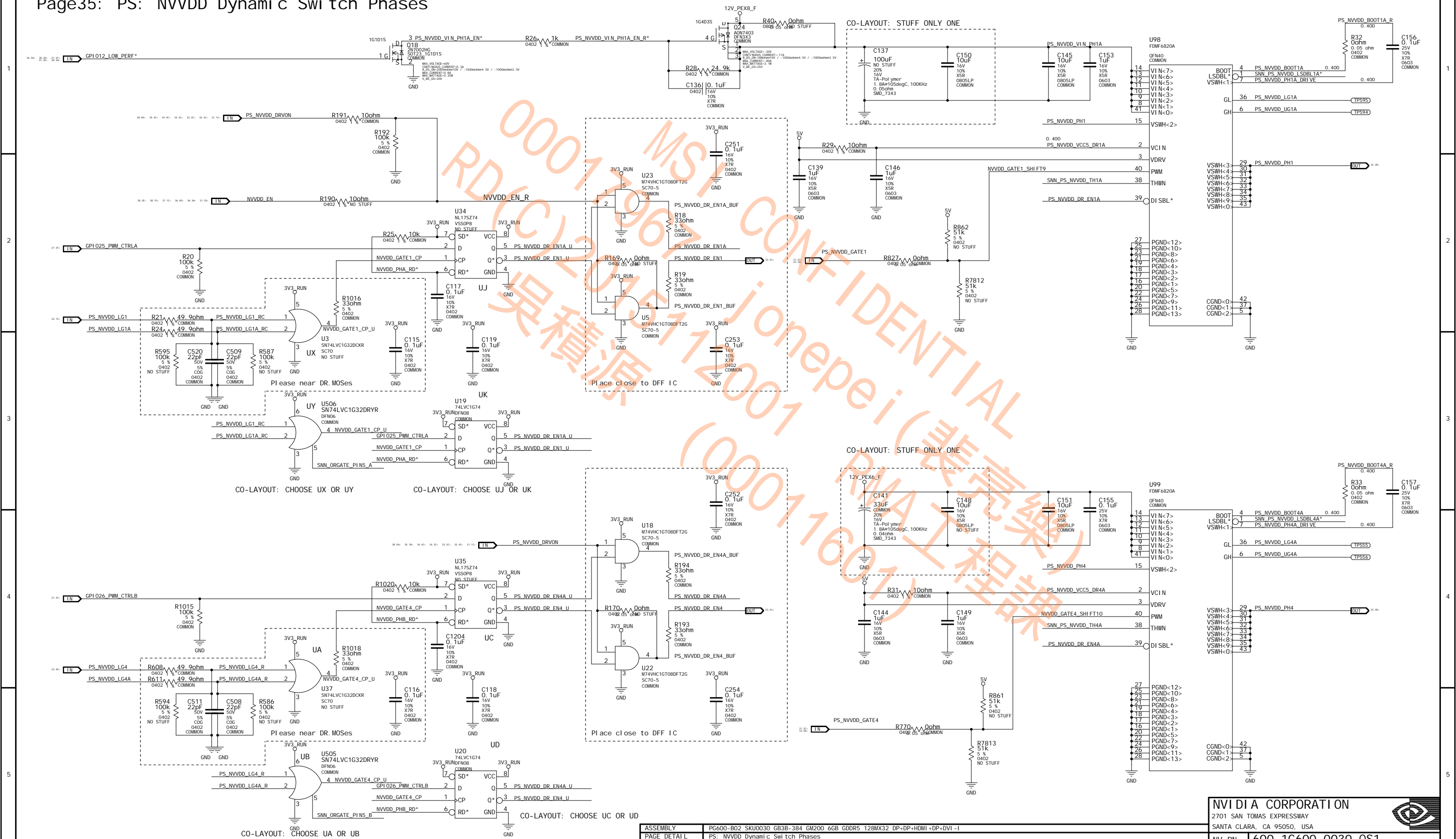
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Page35: PS: NVVDD Dynamic Switch Phases

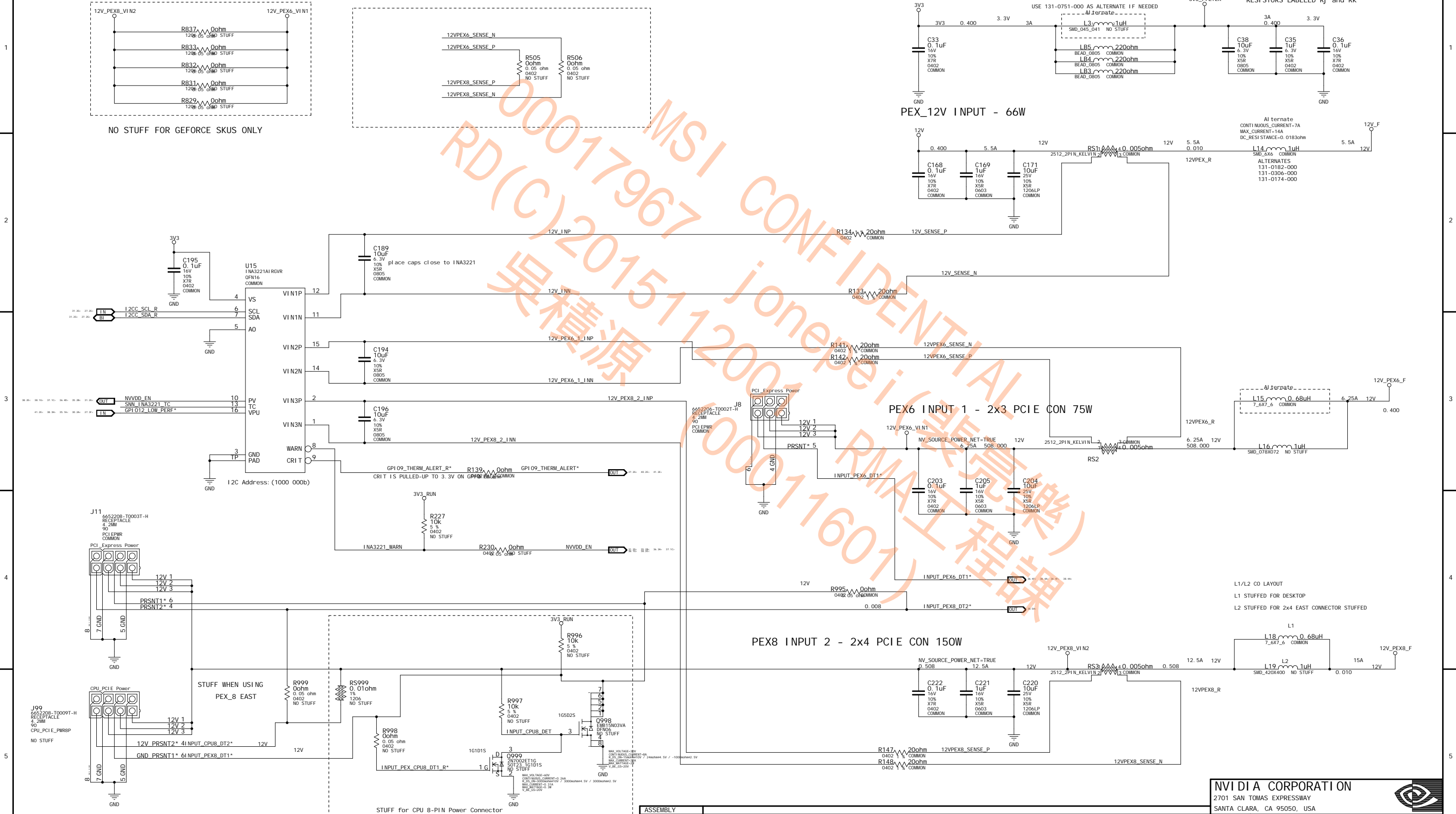


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ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DVI-I
PAGE DETAIL	PS: NVDD Dynamic Switch Phases

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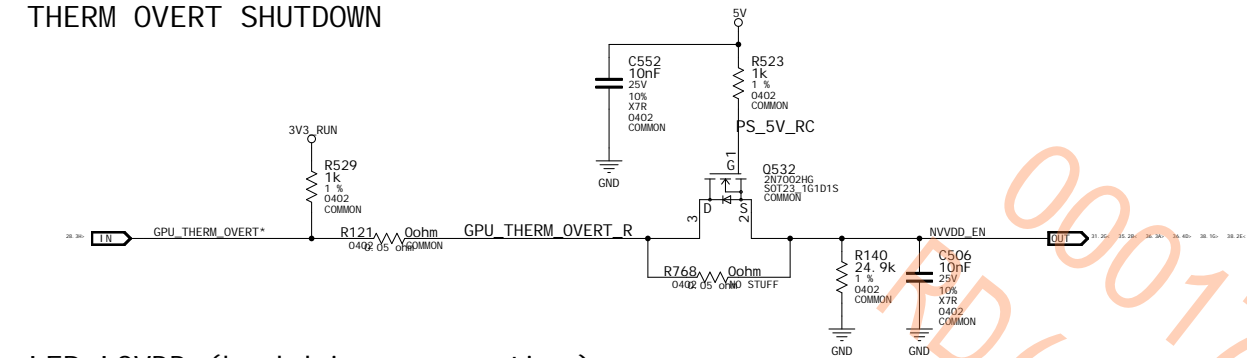
Page36: PS: Inputs, Filtering, and Monitoring



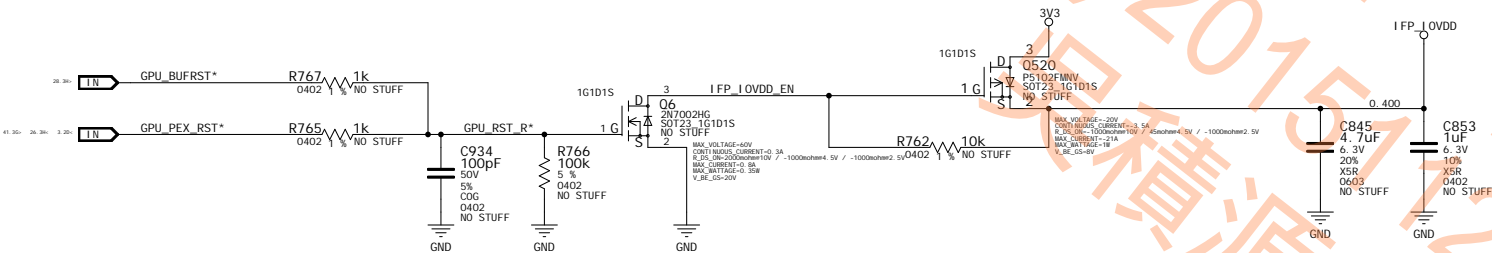
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THERM OVERT SHUTDOWN



I FP_I OVDD (backdrive prevention)



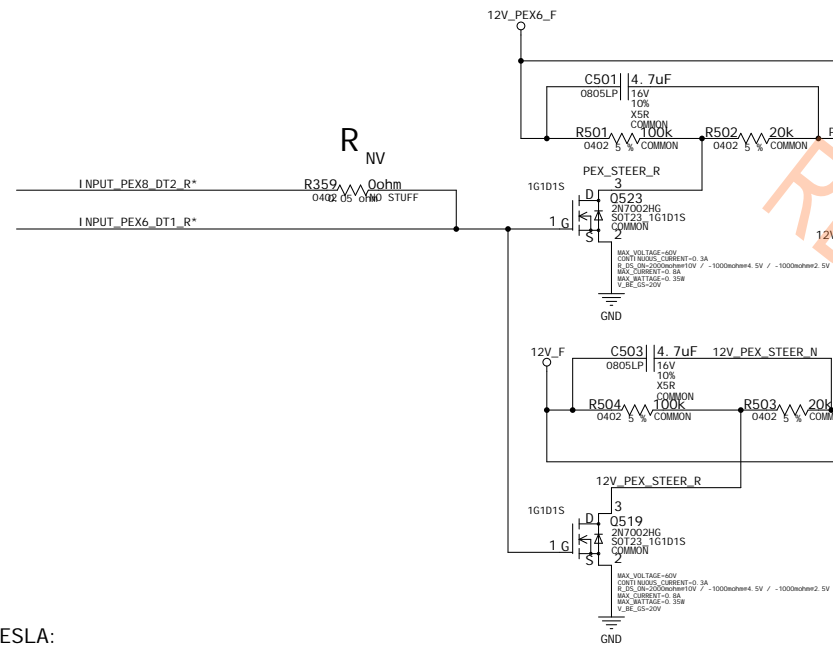
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Page38: PS: 12V Current Steering & Hot Unplug Detect

12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



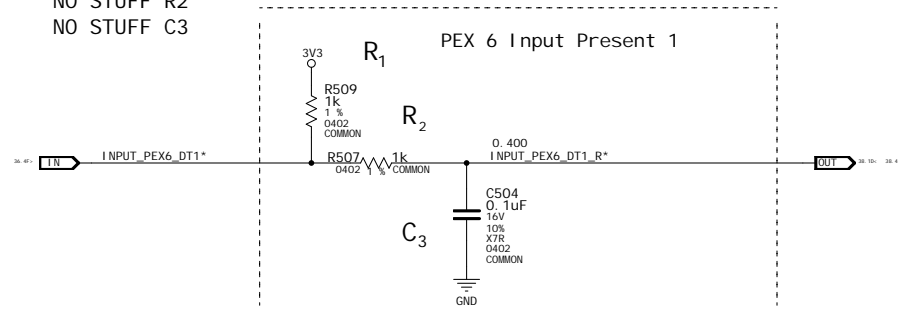
QUADRO/TESLA:

```

PEX 6 INPUT CONNECTOR IS NOT LOADED
PEX 6 INPUT DETECT MUST BE DISABLED
PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING
STUFF Rnv IN STEERING CIRCUIT

NO STUFF R1
NO STUFF R2
NO STUFF C3

```



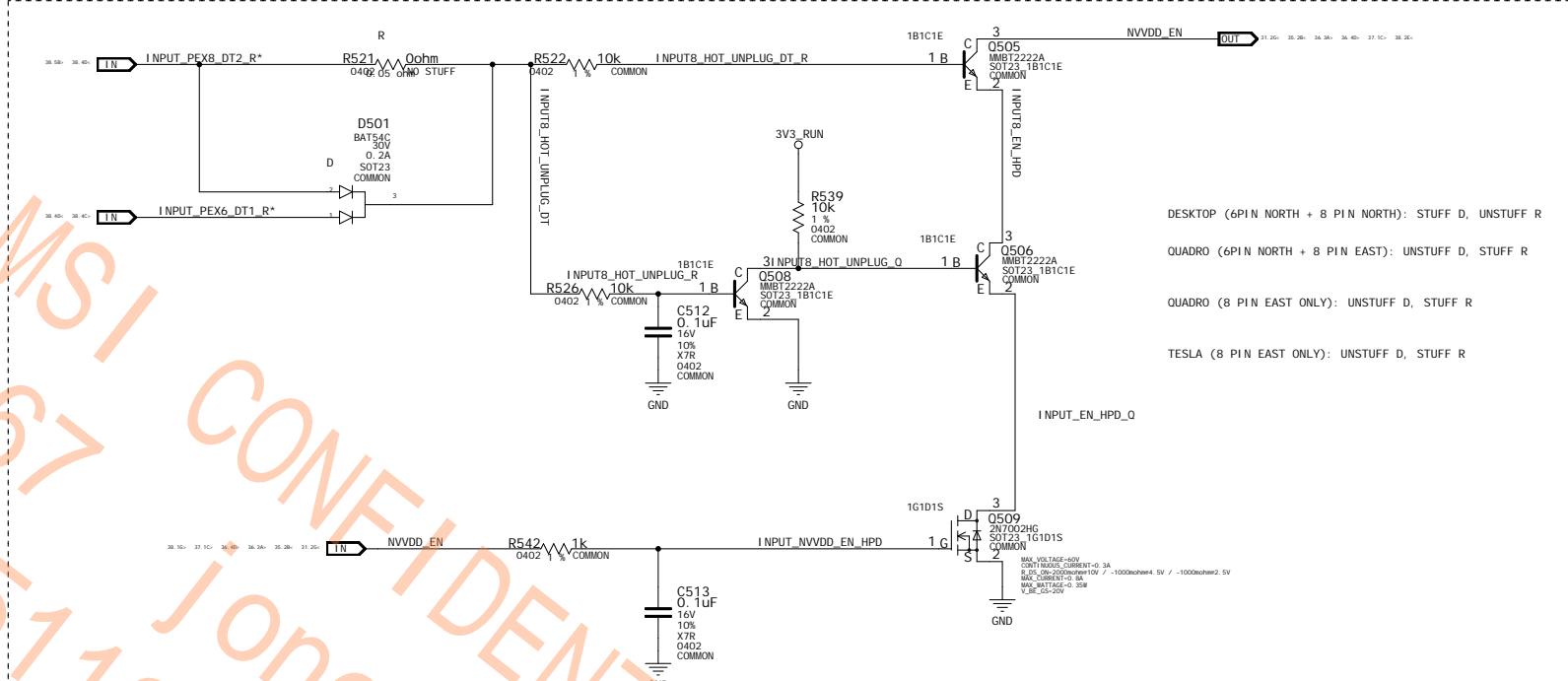
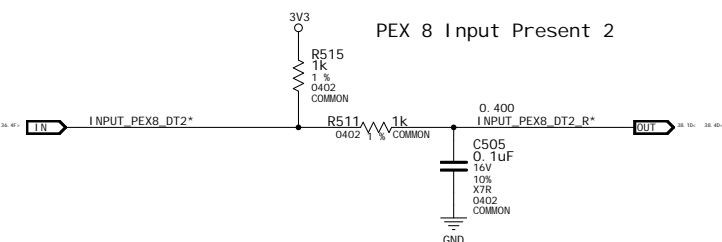
GeFORCE:

```

PEX 6 INPUT CONNECTOR IS LOADED
PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING
NO STUFF Rnv IN STEERING CIRCUIT

STUFF R1
STUFF R2
STUFF C3

```



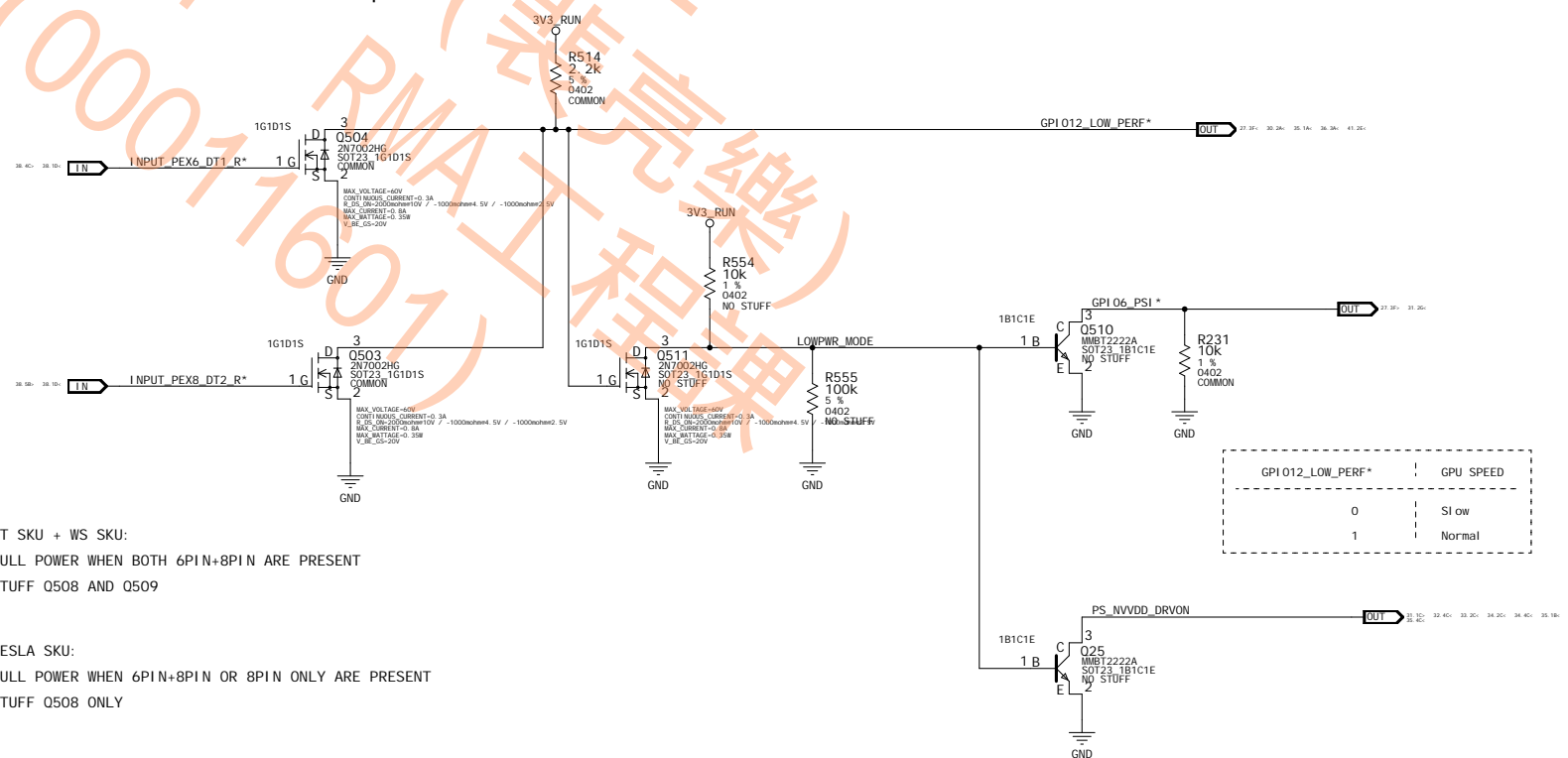
DESKTOP (6PIN NORTH + 8 PIN NORTH): STUFF D, UNSTUFF R

QUADRO (6PIN NORTH + 8 PIN EAST): UNSTUFF D, STUFF R

QUADRO (8 PIN EAST ONLY): UNSTUFF D, STUFF R


TESLA (8 PIN EAST ONLY): UNSTUFF D, STUFF R

PEX Input - Under Power Boot Controls



DT SKU + WS SKU:
FULL POWER WHEN BOTH 6PIN+8PIN ARE PRESENT
STUFF Q508 AND Q509

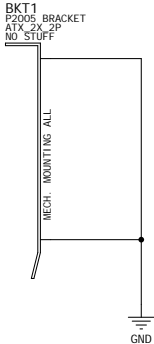
TESLA SKU:
FULL POWER WHEN 6PIN+8PIN OR 8PIN ONLY ARE PRESENT
STUFF Q508 ONLY

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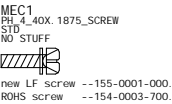
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Brackets:

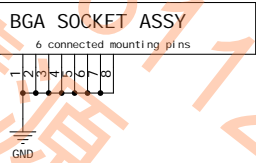
DVI DVI_HDMI_DP : 151-10001-0441-092



Bracket Screw

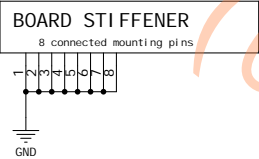


GPU SOCKET



P-Release
MEC7
SOCKET_BGA_GK110
BPI N
NO STUFF

GPU Sti ffener (BRI NG-UP COOLER)



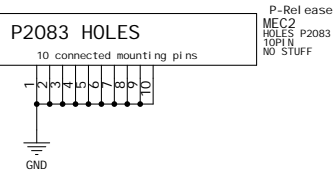
MEC5
GPU STI FFENER_GF100
BPI N
NO STUFF

Sti ffener



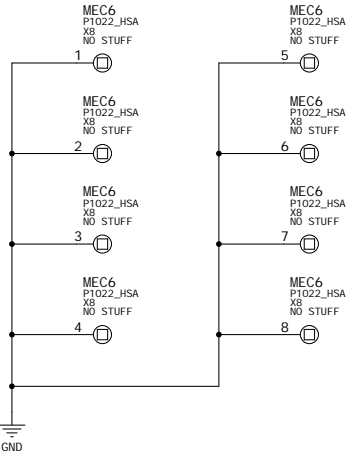
N/A
MECS01
HSB_GK104
NO PIN
NO STUFF

Mechani cal Hol es Symbol



P-Release
MEC2
HOLES P2083
TOP IN
NO STUFF

Bri ng Up Cool er



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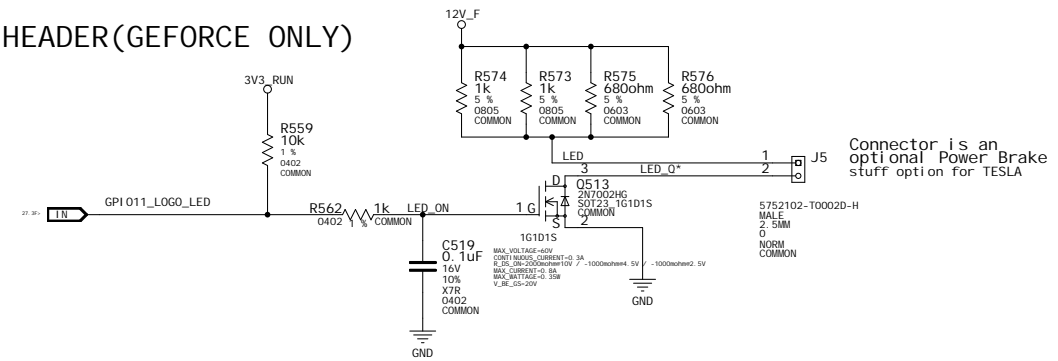
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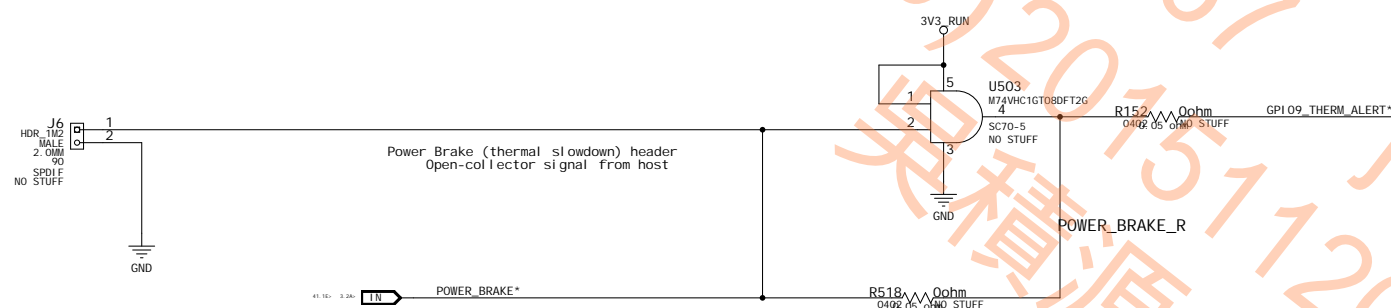
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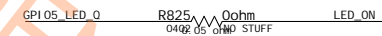


Connector is an optional Power Brake stuff option for TESLA

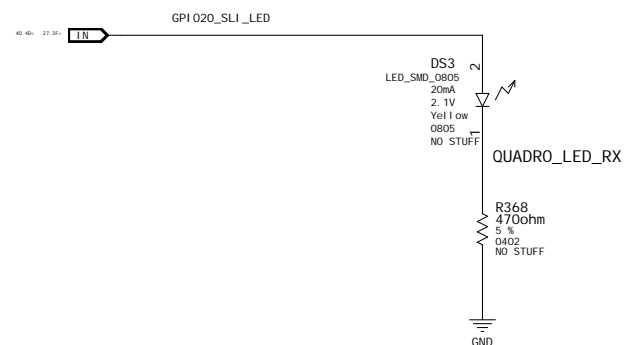
Bypass filter option



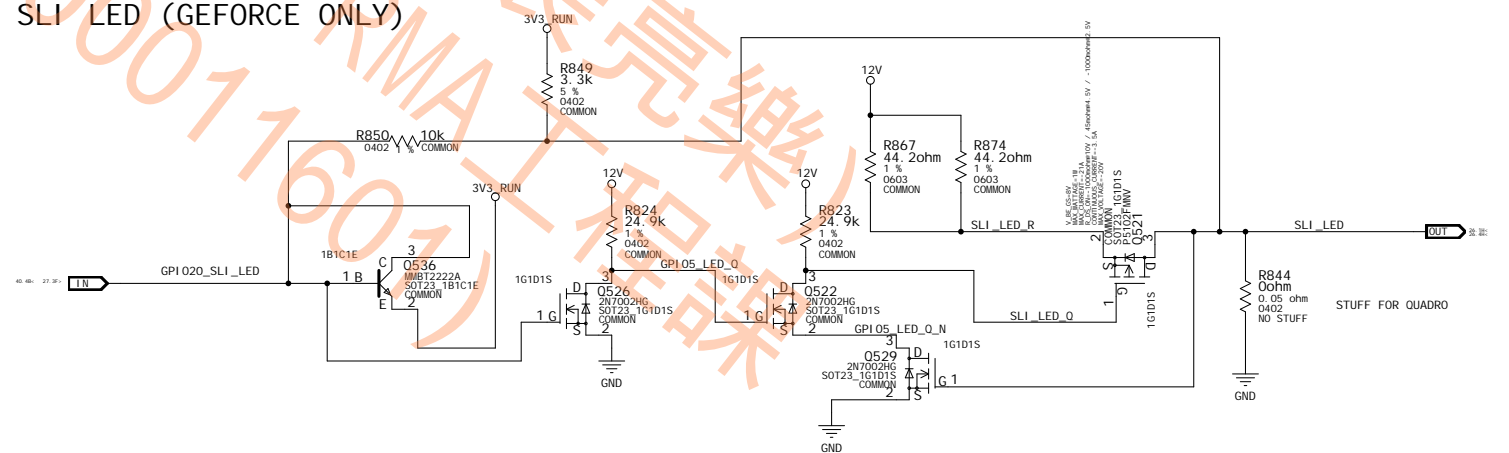
USING GPIO5 TO DIM GEFORCE AND SLI LED



LED FOR QUADRO
PLACE BETWEEN DP Connectors
CONNECTORS



SLI LED (GEFORCE ONLY)



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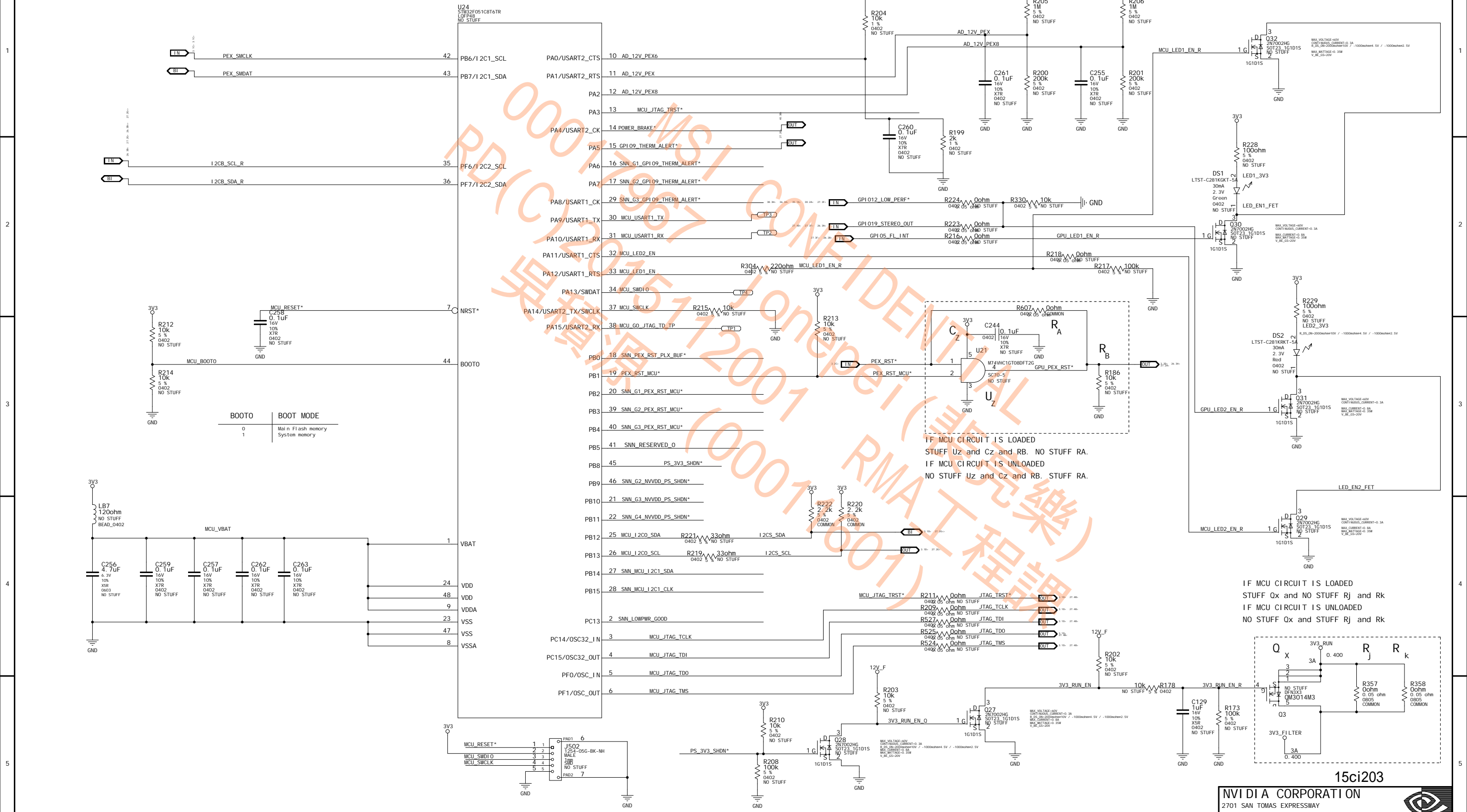
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